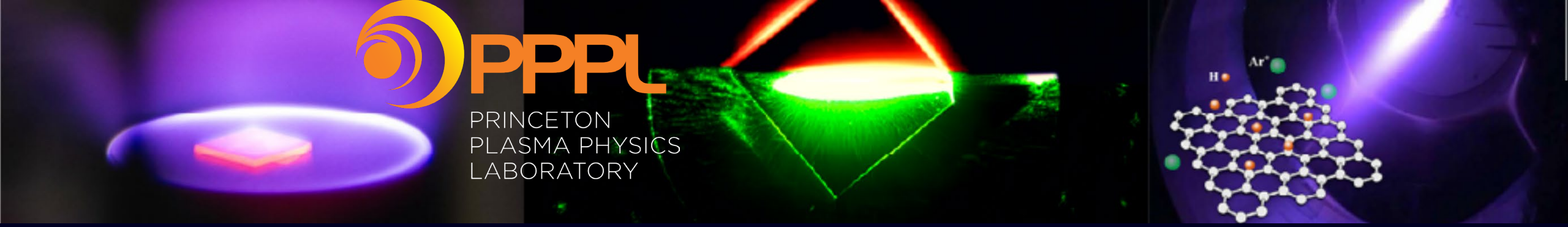

Introduction to Microelectronics Technologies and Industry

Satoshi Hamaguchi

University of Osaka

大阪大学
OSAKA UNIVERSITY

Outline

1. The semiconductor industry
   - overview
   - technology roadmap
   - brief history
2. Outline of chip products: logic, memory, storage,
3. Fundamentals of device physics
4. Fundamentals of Chip Manufacturing
   - Front-end processes (FEOL & BEOL)
   - Back-end processes
5. Summary

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Semiconductor Industry: growth & challenges

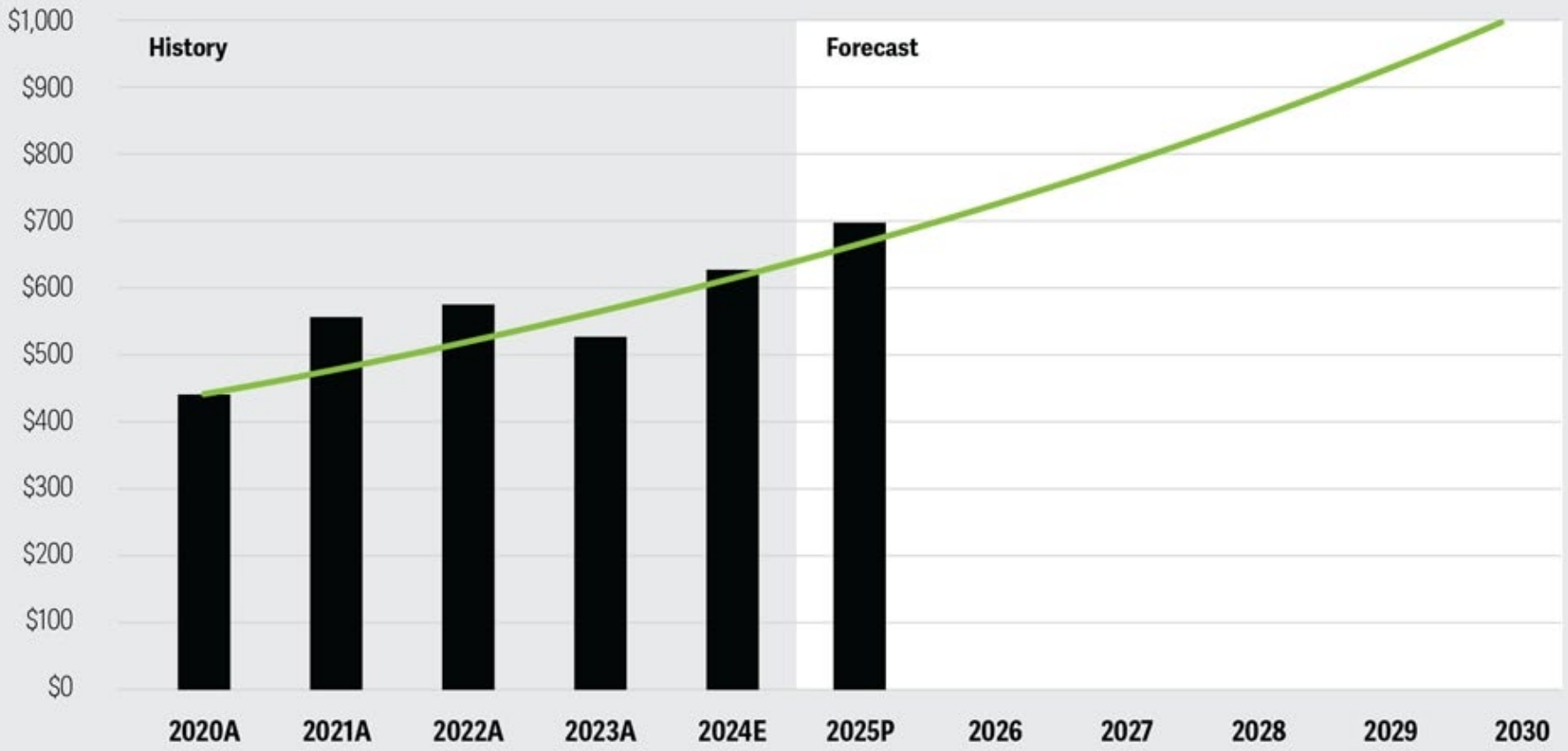
- Continued growth: WW Revenues of $628 (2024) up by 19.1% from $ 527 B (2023)
- The supply chain is global, causing concern on national security issues.
- End of Moore's law; paradigm shift in technology
  - Sizes of some devices are approaching atomic scale
  - Devices with new materials & new 3D structures must be manufactured.
- For the manufacturing of advanced semiconductor products, plasma processing is becoming one of the bottle-neck technologies.

- https://www.idc.com/getdoc.jsp?containerId=IDC_P19632
- https://www.semiconductors.org/global-semiconductor-sales-increase-19-1-in-2024-double-digit-growth-projected-in-2025/

Figure 1

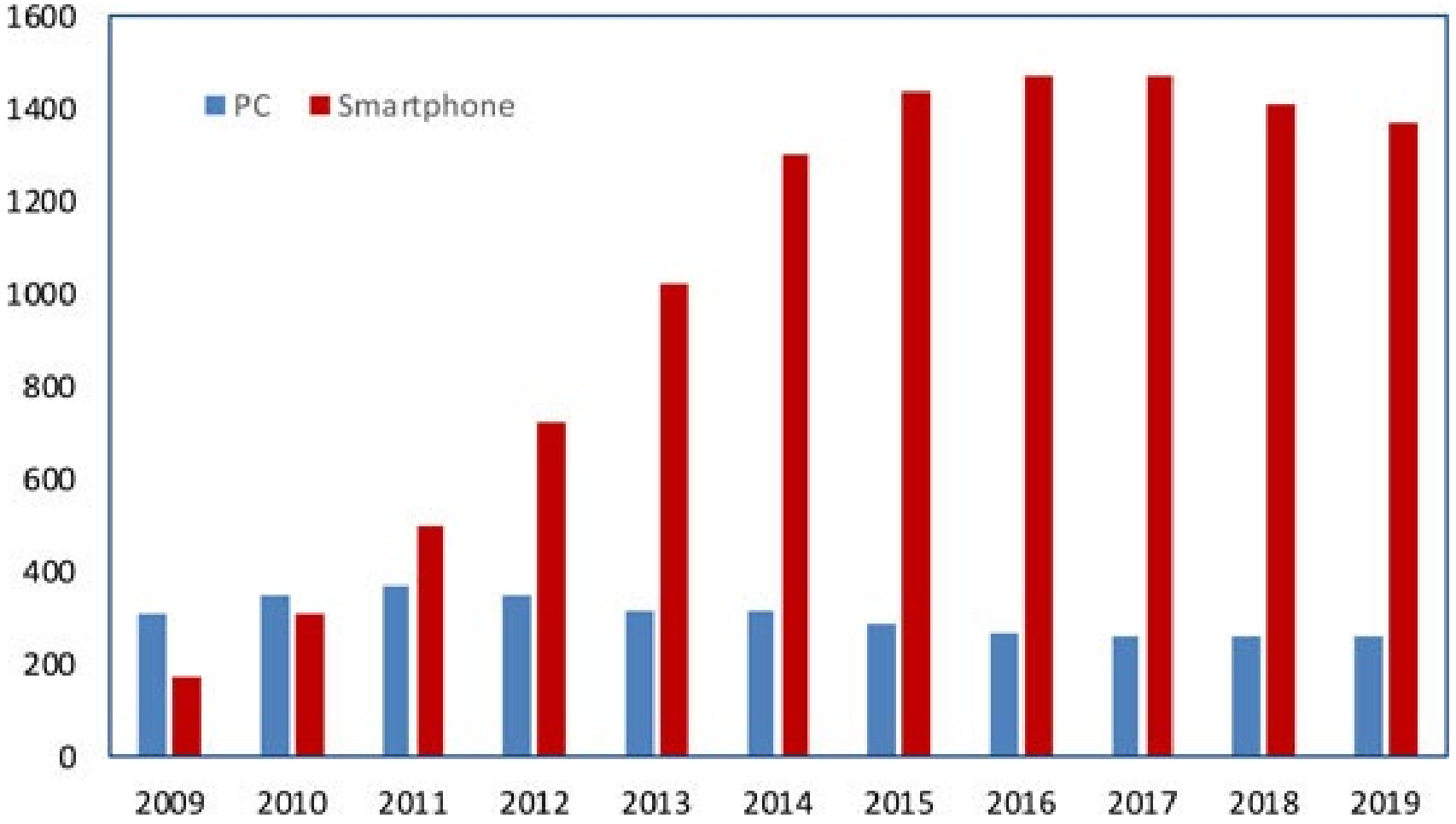
Revenues indicate the possibility of the chip industry hitting US$1 trillion in 2030

The path to $1 trillion in semiconductor revenues ($Billions)



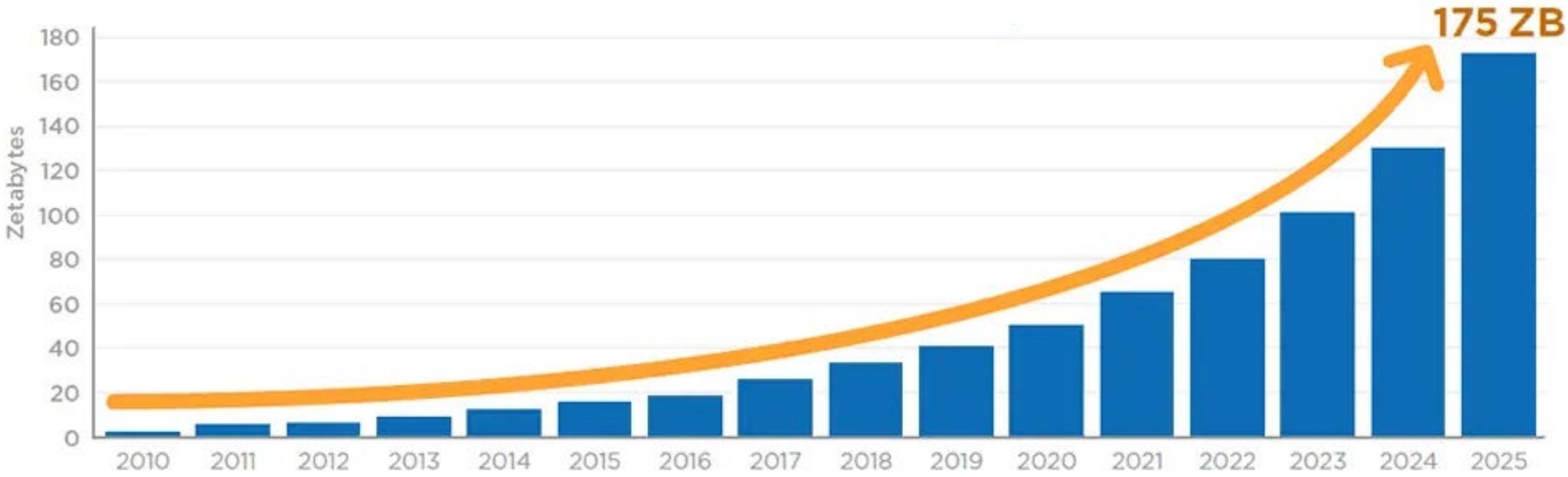
Note: A = Actual, E = Estimate, P = Prediction.
Source: Deloitte analysis and extrapolation based on data from World Semiconductor Trade Statistics.

Global Sales of PCs and Smartphones (Millions of Units)



Published in May 2020 : IMF e-Library
https://www.elibrary.imf.org/view/journals/001/2020/070/article-A001-en.xml

Amount of data created and stored each year

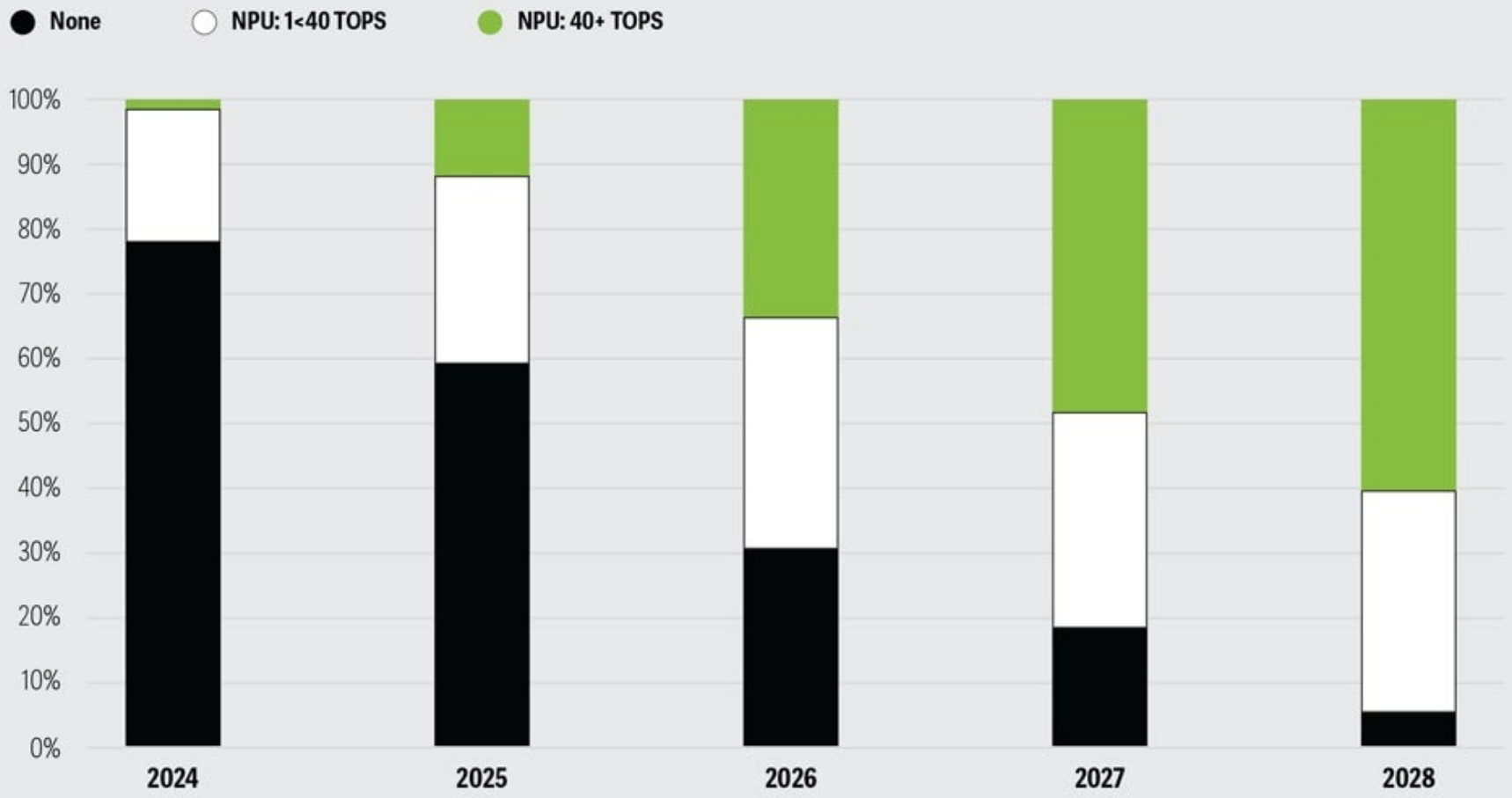


source: IDC Datasphere whitepaper
https://www.i-scoop.eu/big-data-action-value-context/data-age-2025-datasphere/

Figure 4

Almost all PCs are expected to have some gen AI processing—also known as neural processing units (NPUs)—by 2028

Expected sales of NPU-enabled PCs of all PCs worldwide from 2024 to 2028



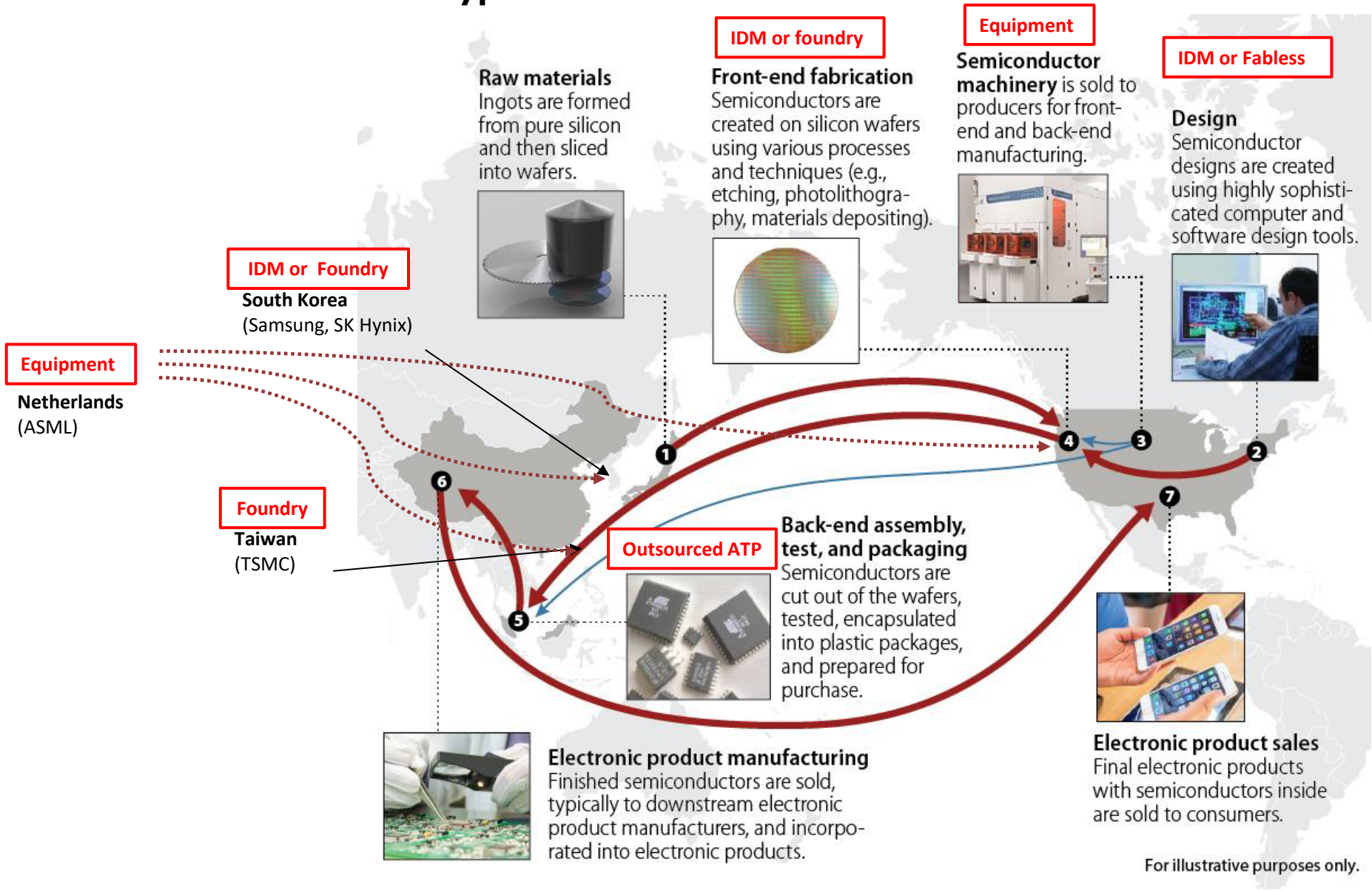
Note: TOPS = trillion operations per second.
Source: International Data Corporation Worldwide Quarterly Personal Computing Device Tracker, September 2024.

AI will drive the future semiconductor industry

- AI data centers
- Edge computing[1)] (Pervasive computing)
- Autonomic computing[2)]

1) "What is the edge computing" https://www.ibm.com/topics/edge-computing
2) Autonomic computing (AC) is distributed computing resources with self-managing characteristics, adapting to unpredictable changes while hiding intrinsic complexity to operators and users (https://en.wikipedia.org/wiki/Autonomic_computing)

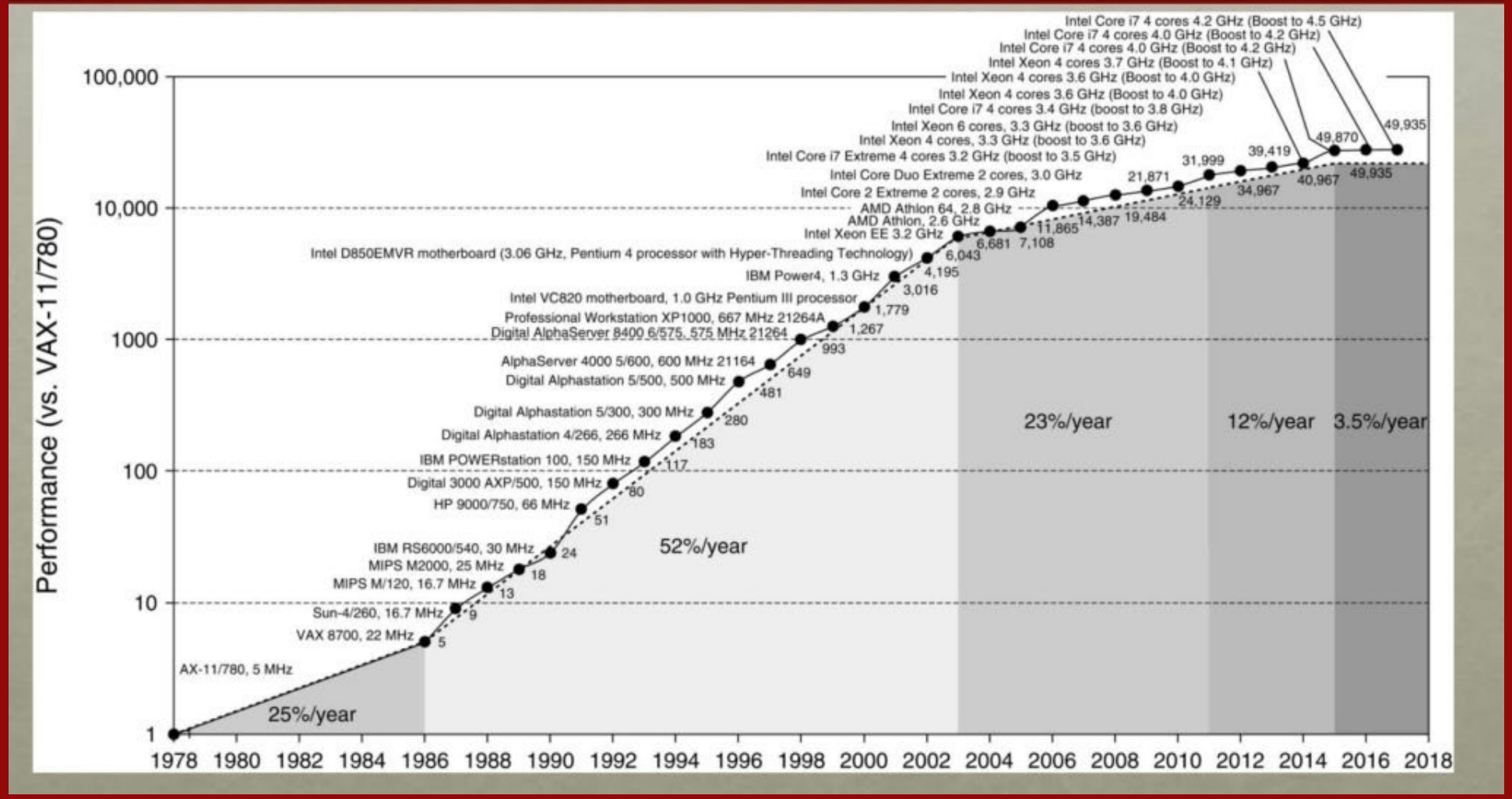
Typical Global Semiconductor Production Pattern



IDM: Integrated Device Manufacture
ATP: Assembly, Test, and Packaging

Source: CRS, adapted from information provided by SIA.

End of Moore's Law



https://www.nextbigfuture.com/2019/02/the-end-of-moores-law-in-detail-and-starting-a-new-golden-age.html

...yet critical applications are also undergoing a paradigm shift

	Compute-centric paradigm	**Data-centric paradigm**
Main Focus:	**Solve differential equations**	**Analyze petabytes of data**
Bottleneck:	***CPU / Memory***	***Storage & I/O***
Typical Examples:	Computational Fluid Dynamics Finite Element Analysis Multi-body Simulations	Search and Mining Analyses of social/terrorist networks Sensor network processing Digital media creation/transmission Environmental & economic modeling

Extrapolation to 2020

(at 90% CGR → need **1.7 PB/sec**)

- **5.6 million HDD**
  - **19,000** sq. ft. !!
  - **25 Megawatts**

(at 90% CGR → need **8.4G SIO/sec**)

- **21 million HDD**
  - **70,000** sq. ft. !!
  - **93 Megawatts**

[Freitas:2008]

"Storage Class Memory - Towards a disruptively low-cost solid-state non-volatile memory" Science & Technology, IBM Almaden Research Center (2013)

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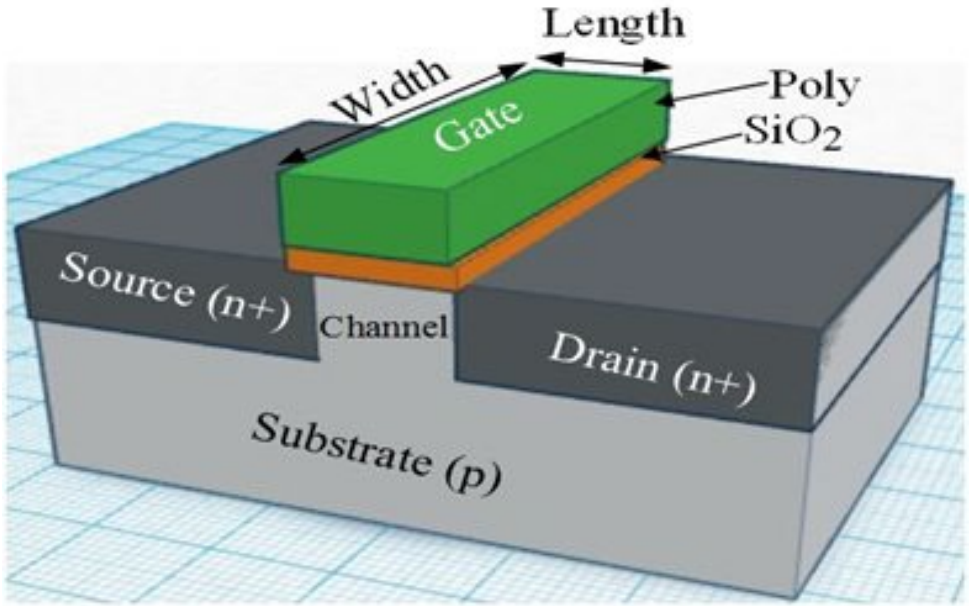
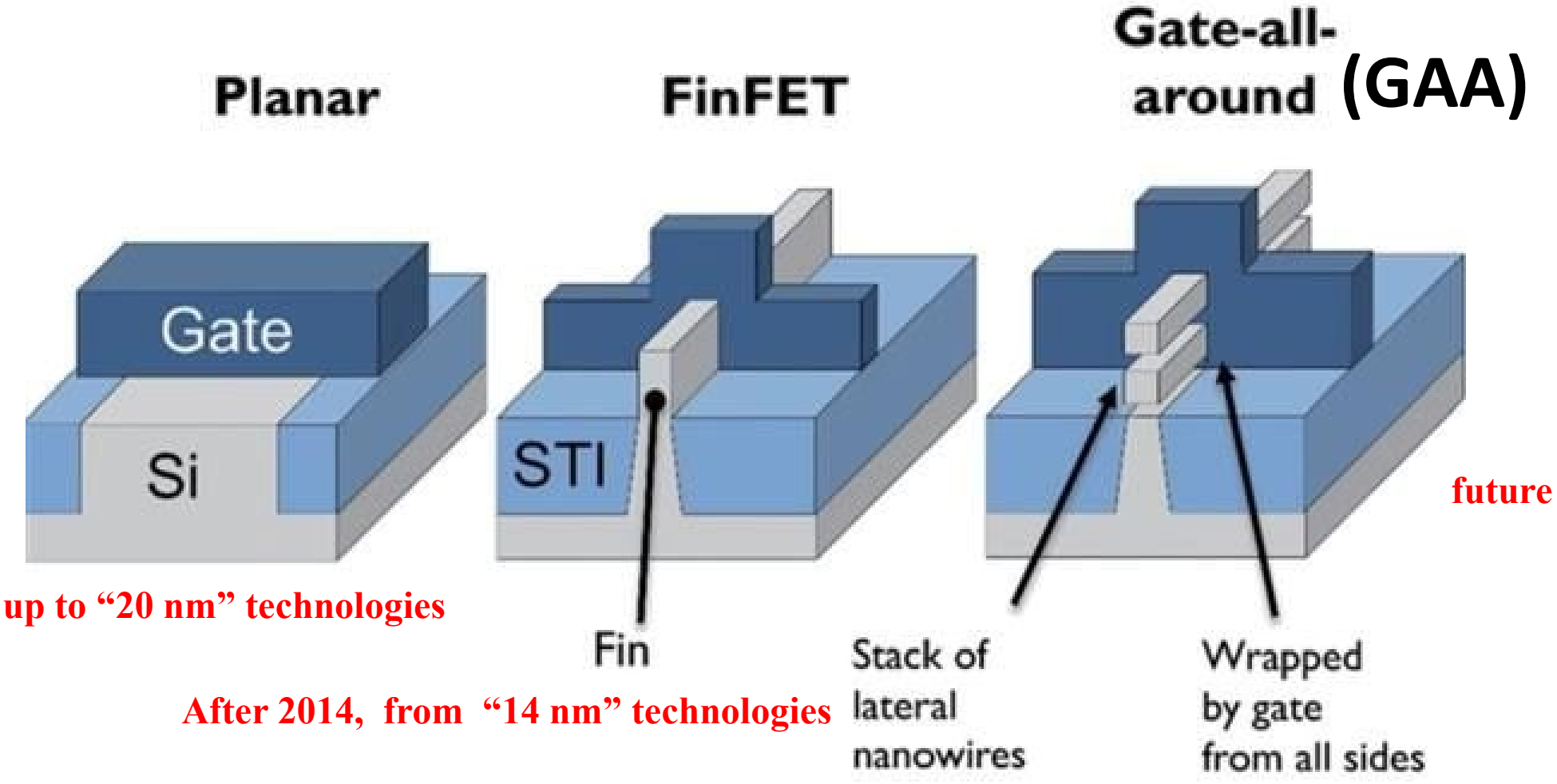
device shapes get more complex



Before 2014, up to "20 nm" technologies

https://www.design-reuse.com/articles/41330/cmos-soi-finfet-technology-review-paper.html

device shapes get more complex



future

Before 2014, up to "20 nm" technologies

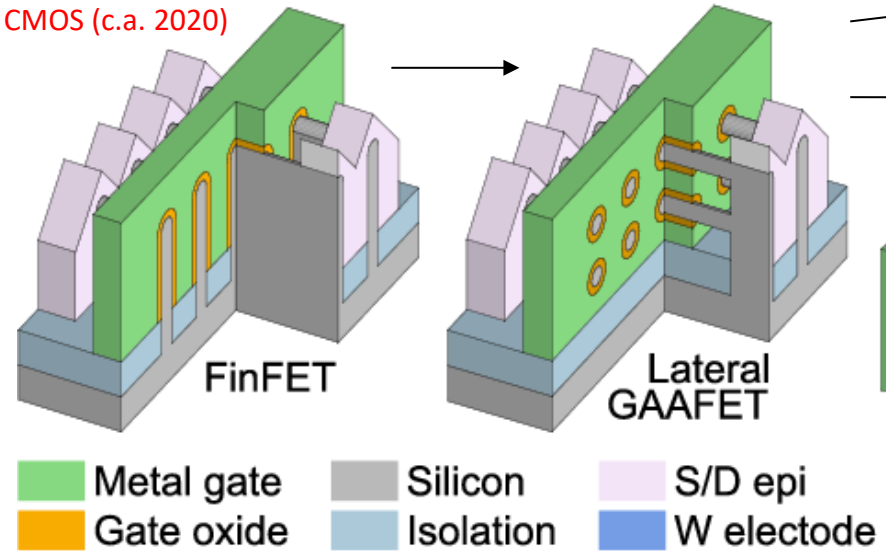
After 2014, from "14 nm" technologies

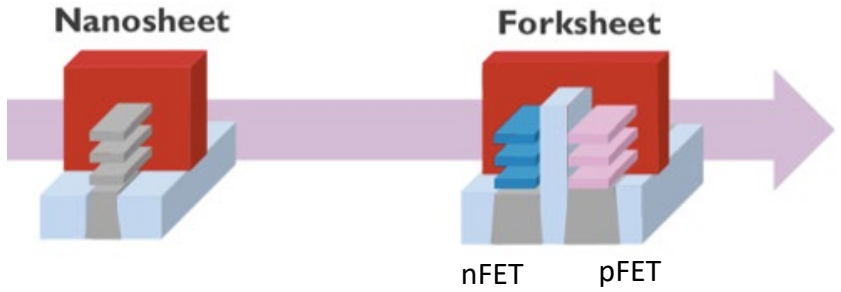
STI: shallow trench isolation

https://www.ednasia.com/all-you-need-to-know-about-gaa-chip-manufacturing-process/

D. Yakimets, et al., IEEE Trans. Electron Devices 62, 1433 (2015).

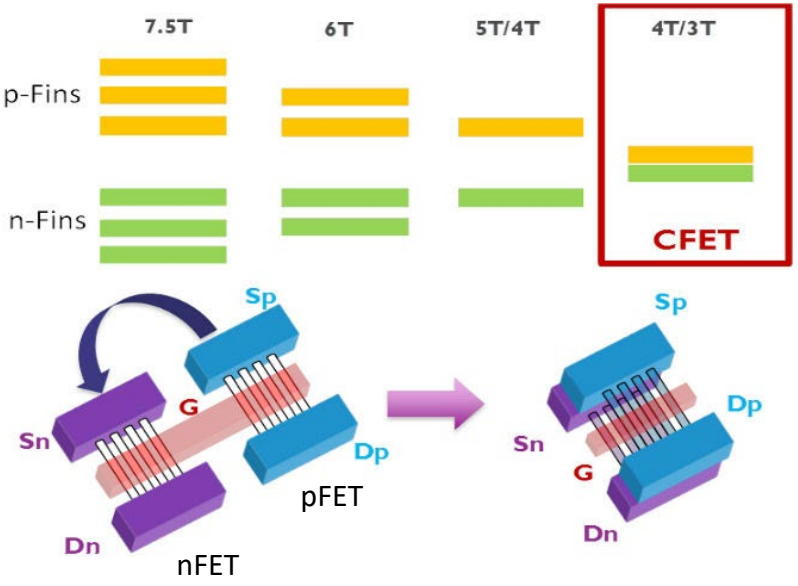
current generation
CMOS (c.a. 2020)

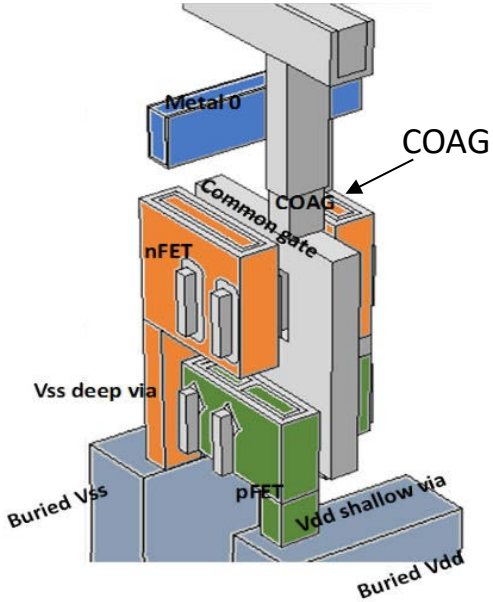




nFET and pFET are placed side by side (CMOS)

Complementary FET (CFET)





COAG: contact-over-active gate

nFET and pFET are placed vertically

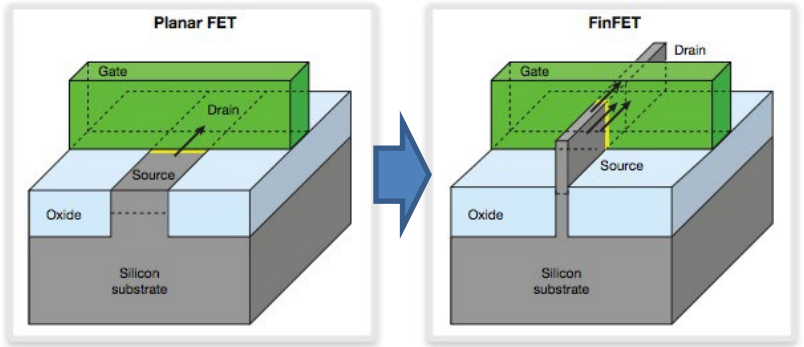
IMEC
https://www.eedesignit.com/fetnodesn3/

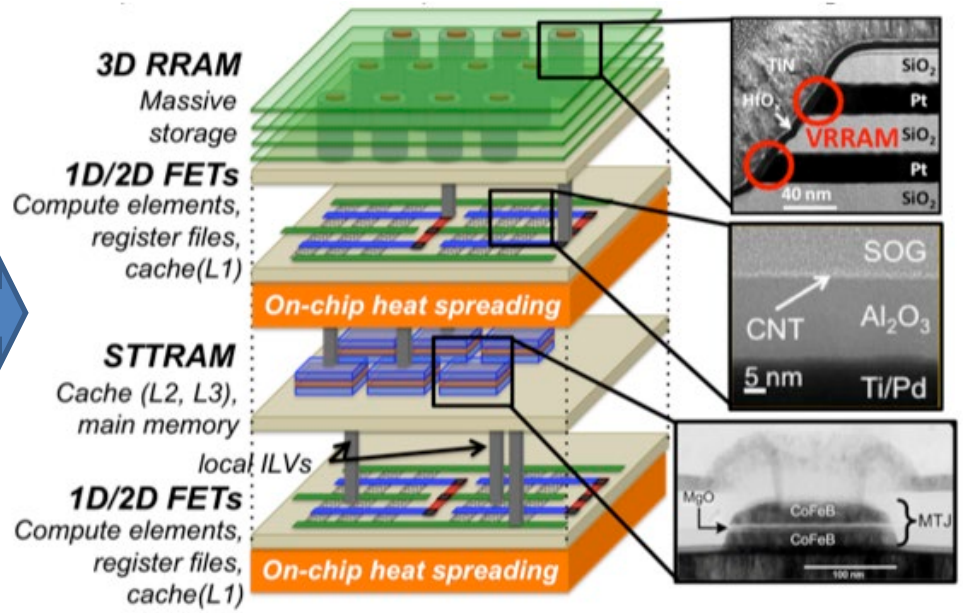
Development of Device Structures

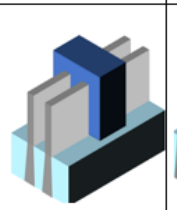
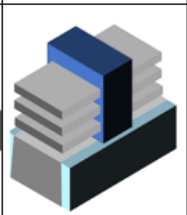
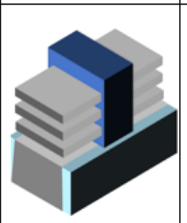
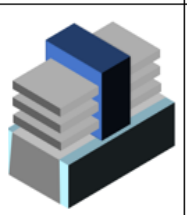
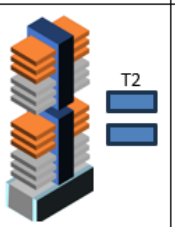
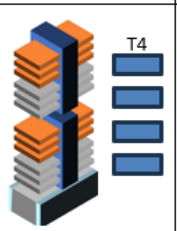
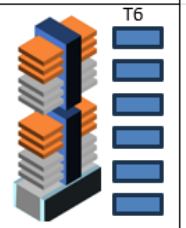
YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	finFET FDSOI	finFET FDSOI	finFET LGAA	finFET LGAA VGAA	VGAA, M3D	VGAA, M3D	VGAA, M3D
							

Figure MM3: Transistor structure roadmap: FDSOI, finFET, lateral nanowire, vertical nanowire, and monolithic 3D.

2015 International Technology Roadmap for Semiconductors (ITRS)



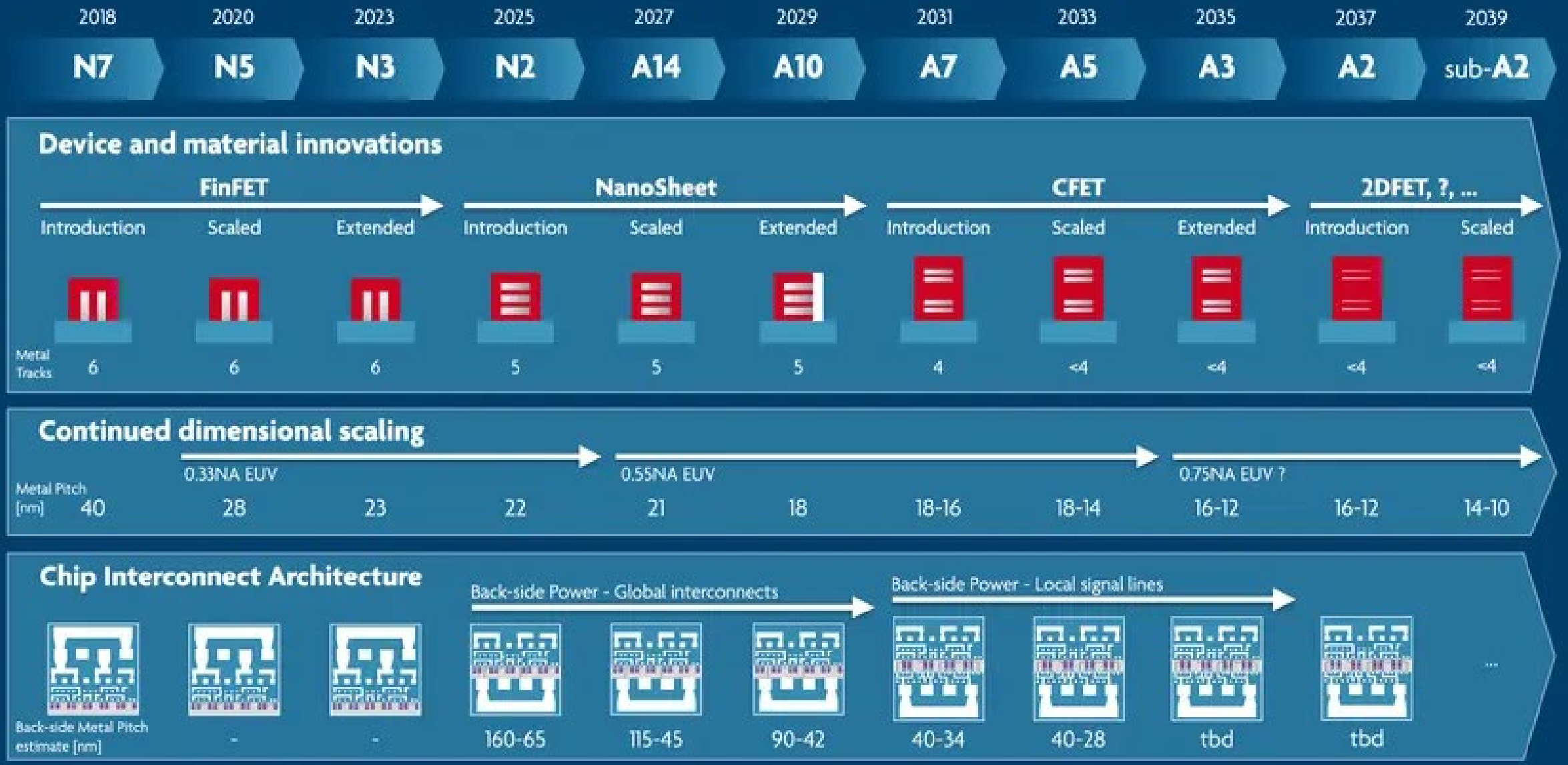


YEAR OF PRODUCTION	2024	2025	2027	2029	2031	2033	2035	2037	2039
	G48M24	G48M22	G48M22	G46M20	G44M18	G44M16	G42M14/T2	G42M14/T4	G42M14/T6
Logic industry "Node Range" Labeling	"3nm" Enhanced	"2nm"	"1.4nm"	"A10 eq"	"A7 eq"	"A5 eq"	"A3.5 eq"	"A2.5 eq"	"A1.8 eq"
Fine-pitch 3D integration scheme	Stacking	Stacking	Stacking	Stacking	CFET	CFET	3DVLSI	3DVLSI	3DVLSI
Logic device structure options	finFET	LGAA	LGAA	LGAA	CFET	CFET	CFET-3D	CFET-3D	CFET-3D
Backside structure options	-	Backside via	Direct contact	Decap+ESD	Active devices	Active devices	Active devices	Active devices	Active devices
Platform device for logic	finFET	LGAA	LGAA	LGAA	CFET	CFET	CFET	CFET	CFET
									
LOGIC DEVICE GROUND RULES									
Mx pitch (nm)	32	24	24	20	18	16	14	14	14
M1 pitch (nm)	32	32	32	46	44	44	42	42	42
M0 pitch (nm)	24	22	22	20	18	16	14	14	14
Gate pitch (nm)	48	48	48	46	44	44	42	42	42
Lg: Gate Length - HP (nm)	16	14	12	12	12	10	10	10	10
Lg: Gate Length - HD (nm)	18	14	12	12	12	10	10	10	10
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	6	6	5	5	4	4	4	4	4
Spacer k value	3.5	3.3	3.0	3.0	2.7	2.7	2.7	2.7	2.7
Contact CD (nm) - finFET, LGAA	20	22	26	24	24	26	24	24	24
Device architecture key ground rules									
Device lateral pitch (nm)	24	26	24	24	22	22	22	22	22
Device gate vertical overhang (nm)	15	15	15	10	10	10	10	10	10
Device height (nm)	48	57	72	64	75	62	60	53	53
FinFET Fin width (nm)	5.0								
Footprint drive efficiency - finFET	4.21								
Lateral GAA vertical pitch (nm)		18.0	17.0	16.0	15.0	14.0	13.0	12.0	12.0
Lateral GAA (nanosheet) thickness (nm)		6.0	6.0	6.0	5.0	4.0	4.0	4.0	4.0
Number of vertically stacked nanosheets on one device		3	4	4	3	3	3	3	3
LGAA width (nm) - HP		30	20	12	30	25	20	15	12
LGAA width (nm) - HD		15	10	6	15	12	10	8	8
LGAA width (nm) - SRAM		7	6	6	6	6	6	6	6
Footprint drive efficiency - lateral GAA - HP		4.41	5.47	4.80	4.57	4.24	4.00	3.68	3.43
Device effective width (nm) - HP	101.0	216.0	208.0	144.0	210.0	174.0	144.0	114.0	96.0
Device effective width (nm) - HD	101.0	126.0	128.0	96.0	120.0	96.0	84.0	72.0	72.0
PN seperation width (nm)	45	40	30	20					
CFET PN seperation vertical space (nm)					30	20	20	15	15

Device Architecture and Ground Rules Roadmap for Logic Devices.

Note: GxxMxx/Tx notation refers to Gxx: contacted gate pitch, Mxx: tightest metal pitch in nm, Tx: number of tiers. This notation illustrates the technology pitch scaling capability. On top of pitch scaling there are other elements such as cell height, number of stacked devices, DTCO constructs, 3D integration, etc. that define the target area scaling (gates/mm2). LGAA—lateral gate-all-around-device (GAA), CFET (Complementary Field Effect Transistor), 3DVLSI—fine-pitch 3D logic sequential integration.
(https://irds.ieee.org/images/files/pdf/2024/2024IRDS_MM.pdf)

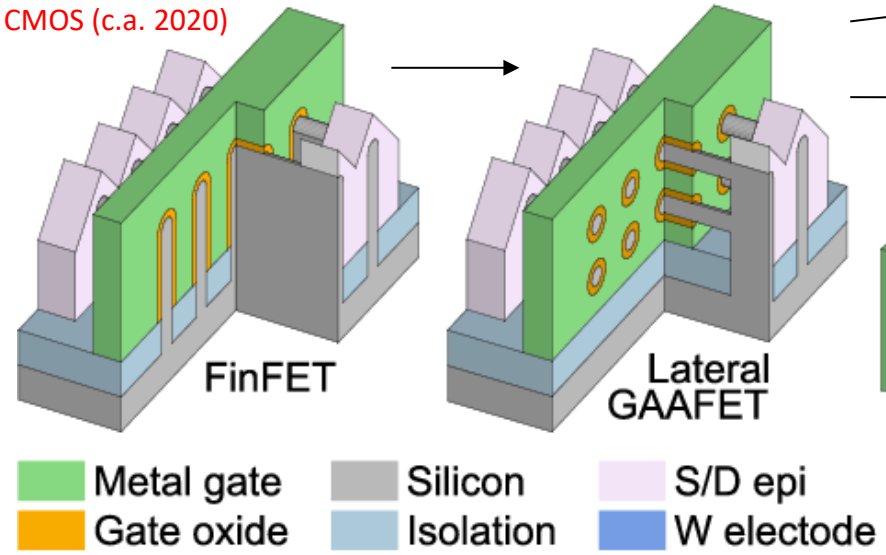
Options extending the roadmap

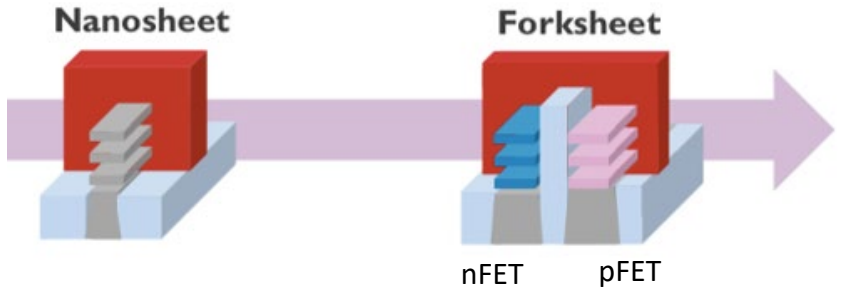


https://www.imec-int.com/en/articles/introducing-2d-material-based-devices-logic-scaling-roadmap

D. Yakimets, et al., IEEE Trans. Electron Devices 62, 1433 (2015).

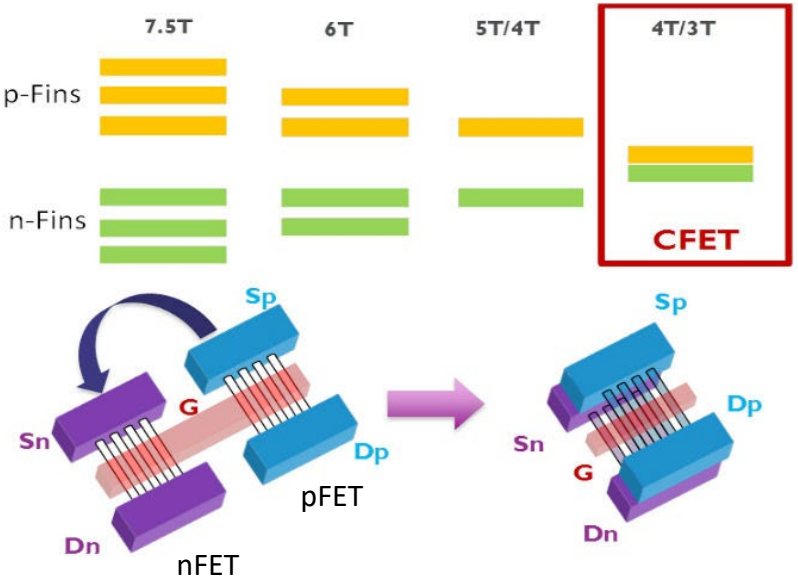
current generation
CMOS (c.a. 2020)

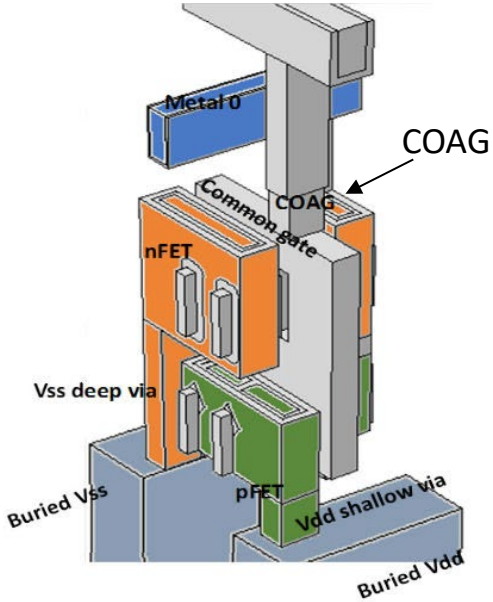




nFET and pFET are placed side by side (CMOS)

Complementary FET (CFET)





COAG: contact-over-active gate

nFET and pFET are placed vertically

IMEC
https://www.eedesignit.com/fetnodesn3/

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Brief History of IC

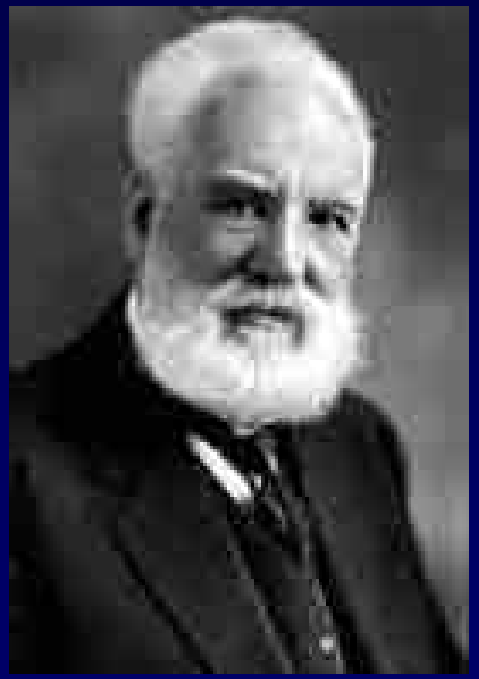
How were the Semiconductor Industry and Silicon Valley born?

New technologies are driven by “Needs”

Necessity is the mother of invention (Plato)

- AT&T(America Telephone & Telegram) in the late 19 Century

— Monopoly of the telephone business due to the patent by Alexander Graham Bell（1876）



Alexander Graham Bell

AT&T HQ in 1958

Loss of telephone monopoly by AT&T

- Problem at 1894 : AT&T

— Expiration of Bell's telephone patent: competition in the telephone business with other companies

- Problem at 1895 : Bologna, Italy

— Invention of radio transmission by Guglielmo Marconi

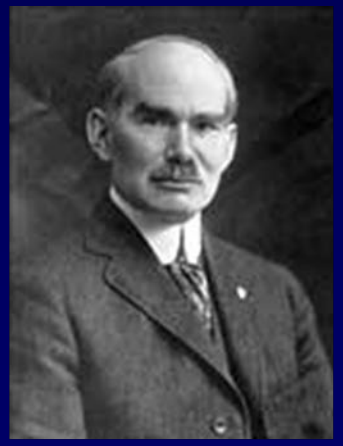
— 1897 : Establishment of Marconi Wireless Telegraph Company : the age of wireless telecommunication

- Strategy of AT&T (1907)

— Plan to build the first transcontinental phone line

— Problem: signal needs to be amplified

— Solution: bought the patent of a triode vacuum tube by Lee De Forest (1906) and started to develop amplifiers.



American Inventor: Lee De Forest

triode vacuum tube amplifier

- 1909 : Announcement by Vail (president of AT&T) of the plan to build the first transcontinental telephone line
- 1914: Completion of the transcontinental line

Theodore Vail (President of AT&T) making long-distance phone call, 1915, Courtesy AT&T

- 1925：Bell Laboratories became a subsidiary company of AT&T
  （number of employees = 3,600, annual budget 12 million dollars: the largest R&D organization in the US by then）

— Objectives： to solve all technical problems for telephone lines in the US

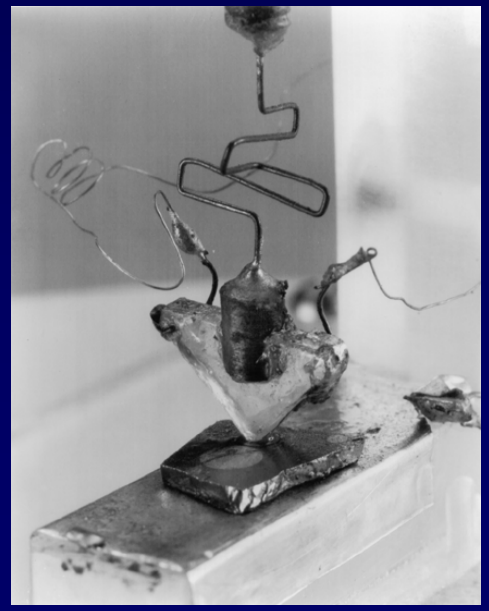
MURRAY HILL, NJ - MARCH 13, 1942: Bell Telephone Laboratory, Murray Hill, New Jersey. Main group from acoustics laboratory roof. Gottscho-Schleisner, Inc./Courtesy Library of Congress Prints and Photographs Division Washington, D.C., call no. LC-G612- 42005

- Big Problem of telephone lines then：vacuum tubes have low reliability and large power consumption
- In 1936, Mervin Kelly became Research Director of Bell Laboratories and, after the WWII, formed a Solid State Physics group (led by W. Shockley) to develop solid-state amplifiers.

Mervin Kelly: director 1936-50, president of Bell Labs 1951-59

- In the Solid State Physics Group of Bell Labs led by William Shockley, experimentalist Walter Brattain and theorist John Bardeen invented a transistor. The Nobel Prize in Physics was granted to Bardeen, Brattain, and Shockley in 1956.

— The team applied quantum mechanics, which was just born in the 1930s, to the development of solid-state devices



pnp point-contact
germanium transistor

Bardeen, Shockley, and Brattain

- AT&T replaced all vacuum-tube-based signal amplifiers with those with transistors in the 1950s and made the system work without switchboard operators.

- Transistors are in high demand for military use：

  — US semiconductor companies did not show much interest in civilian applications.

The first commercial transistor（1949）

The first transistor radio
Regency T1（1954）
（Co-produced by Regency and
Texas Instrument）

Despite its very successful sales, the company stopped production in 1955 in order to focus on other products.

Masaru Ibuka, left, with Akio Morita, Sony Corp.

Tokyo Telecommunication Engineering Co. (which later became SONY) entered the US market for transistor radios after the retreat of T1 and became very successful.

Birth of Silicon Valley

- In 1955, Shockley left Bell Labs and established Shockley Semiconductor in Mountain View, Ca, to develop and manufacture new semiconductor devices.

- In 1957, 8 young scientists (“the Traitorous Eight”) left Shockley Semiconductor and established Fairchild Semiconductor.

- In 1960, Shockley Semiconductor was bought by Clevite Transistor .

Invention of IC（Integrated Circuits）

- In 1957, 8 former Shockley Semiconductor scientists established Fairchild Semiconductor. The 3rd company in the current Silicon Valley.
- In 1959, Robert Noyce of Fairchild Semiconductor invented ICs. (The first IC patent in 1961)
- Around the same time（1958）, Jack Kilby of Texas Instruments (TI) independently invented IC.

The first IC of TI

Fairchild Semiconductor & Intel

- Fairchild Semiconductor grew rapidly in the business of developing and manufacturing ICs. The number of employees grew from 12 to 12,000.
- Noyce introduced Californian style management: casual atmosphere in business.
- Many of co-founders of Fairchild Semiconductor left the company and built their own companies, which became the base of the present-day Silicon Valley. (Fairchildren)
- In 1968, Robert Noyce and Gordon Moore left Fairchild and founded Intel.
- Other include National Semiconductors and Advanced Micro Devices.

Success of Transistors & IC development

- Needs → long-distance telephone line solid-state devices
- Method of development
  - The latest theory of fundamental science（quantum mechanics）
  - Systematic search of materials
- Development of the market
  - Technological innovation (e.g., invention of IC) and market development by Fairchild & Intel

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Types of Semiconductors

Digital

Memory

DRAM

Volatile Memory - loses data when power is lost.

NAND

Non-Volatile Memory, slower & stores less data

Logic

GPUs

Processes many tasks at once. Well suited for graphics and AI.

CPUs

Gives directions to other chips. Processes one task at a time.

ASICs

Designed for one specific purpose. AI accelerators for example.

FPGAs

Can be reprogrammed after manufacturing.

SoCs

Combines other chips onto one chip. Include memory, CPU, and GPU

Analog

Processes continuous signals such as temperature, sound, and light

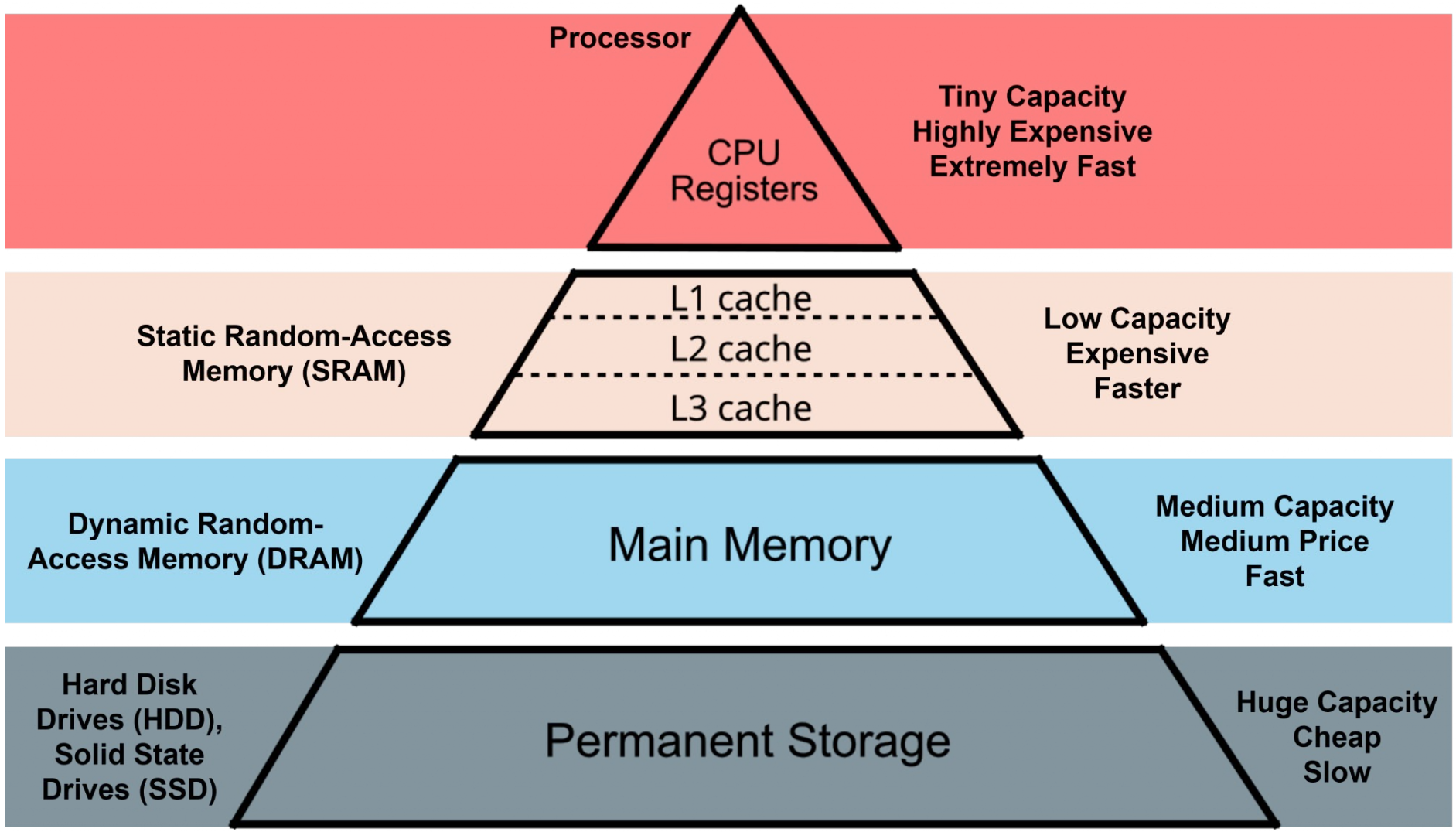
Signal

Measure real-world signals & convert to data

Power

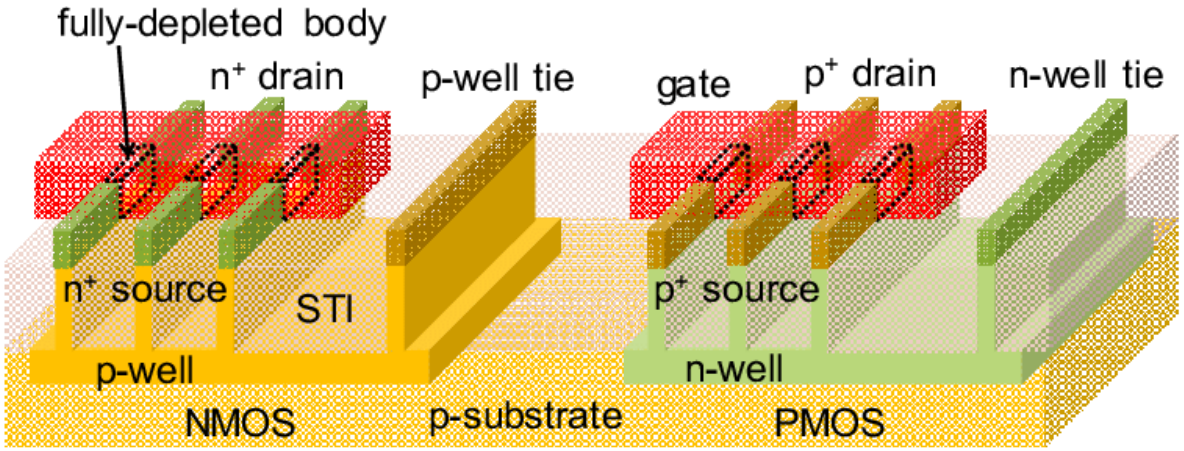
Manages power in electronics: switches, battery managment

https://images.app.goo.gl/HvMb474o8p6ARg1u9

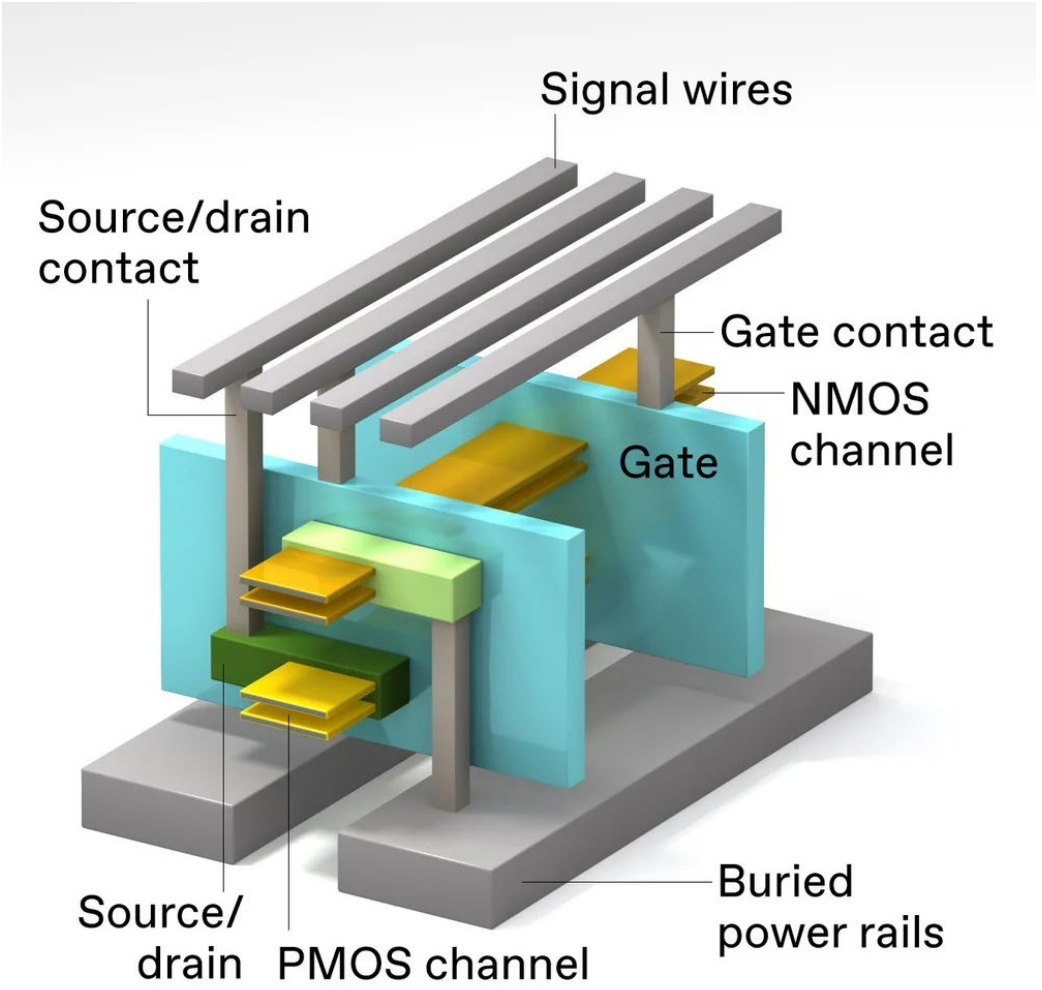

Processor
CPU Registers
Tiny Capacity
Highly Expensive
Extremely Fast
Static Random-Access Memory (SRAM)
L1 cache
L2 cache
L3 cache
Low Capacity
Expensive
Faster
Dynamic Random-Access Memory (DRAM)
Main Memory
Medium Capacity
Medium Price
Fast
Hard Disk Drives (HDD), Solid State Drives (SSD)
Permanent Storage
Huge Capacity
Cheap
Slow

Future CMOS? 3D-stacked CMOS

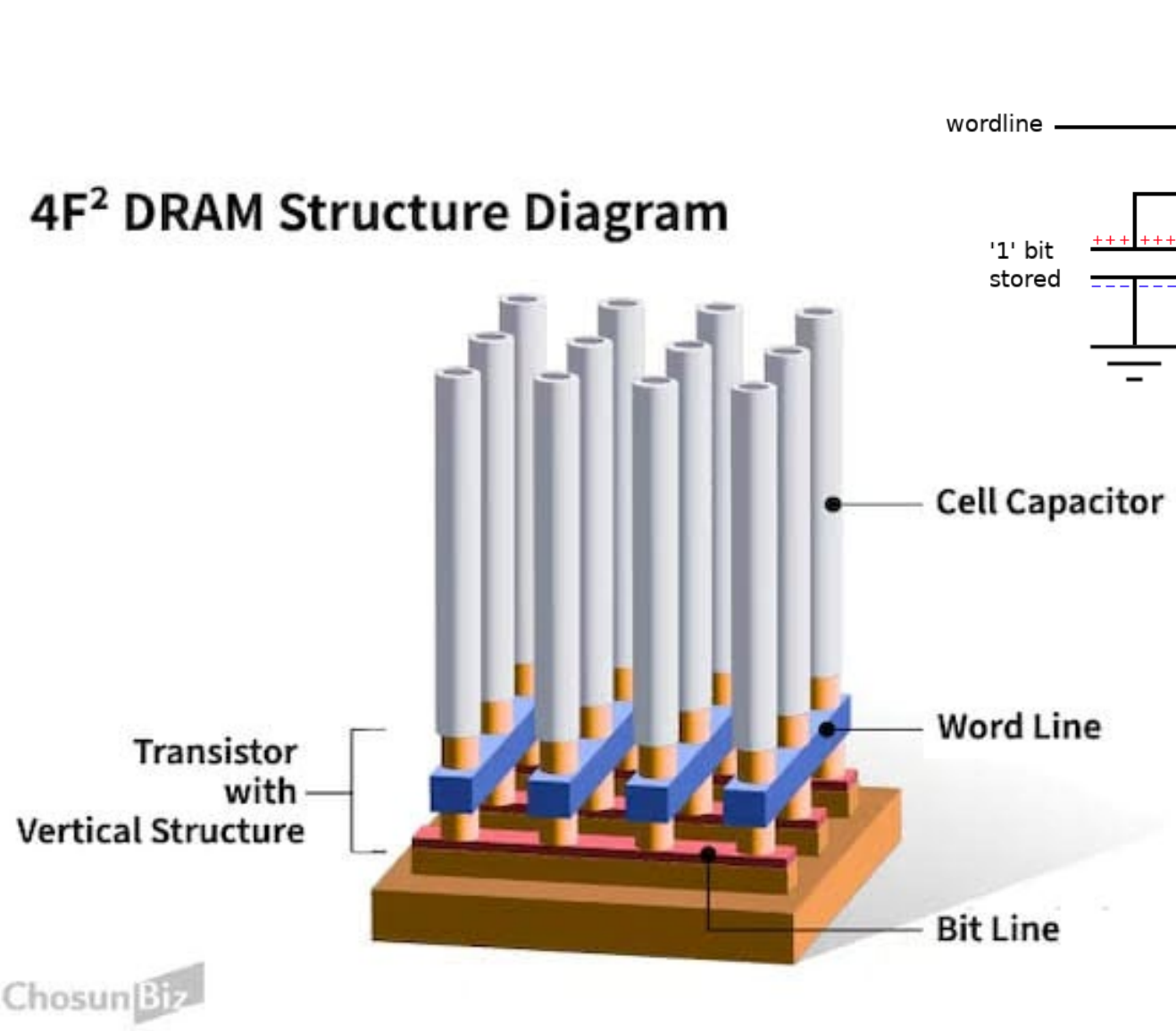
FinFET CMOS: current generation

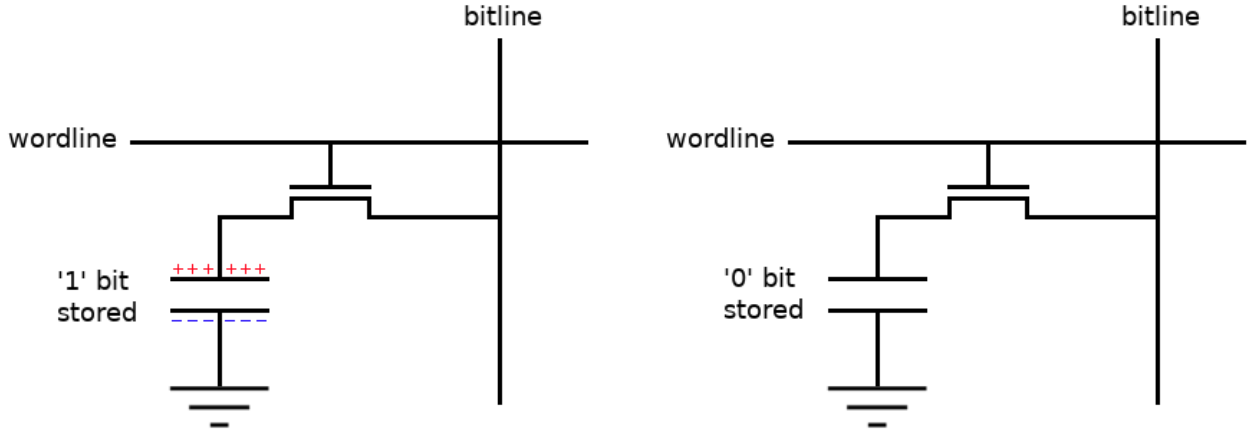


https://www.researchgate.net/publication/324608238/figure/download/fig1/AS:617287212097542@1524184148757/Fully-depleted-bulk-CMOS-finFETs.png



https://spectrum.ieee.org/media-library/orange-elongated-blocks-connect-to-several-narrower-blocks-of-a-variety-of-colors.jpg?id=30542266&width=1000&quality=85





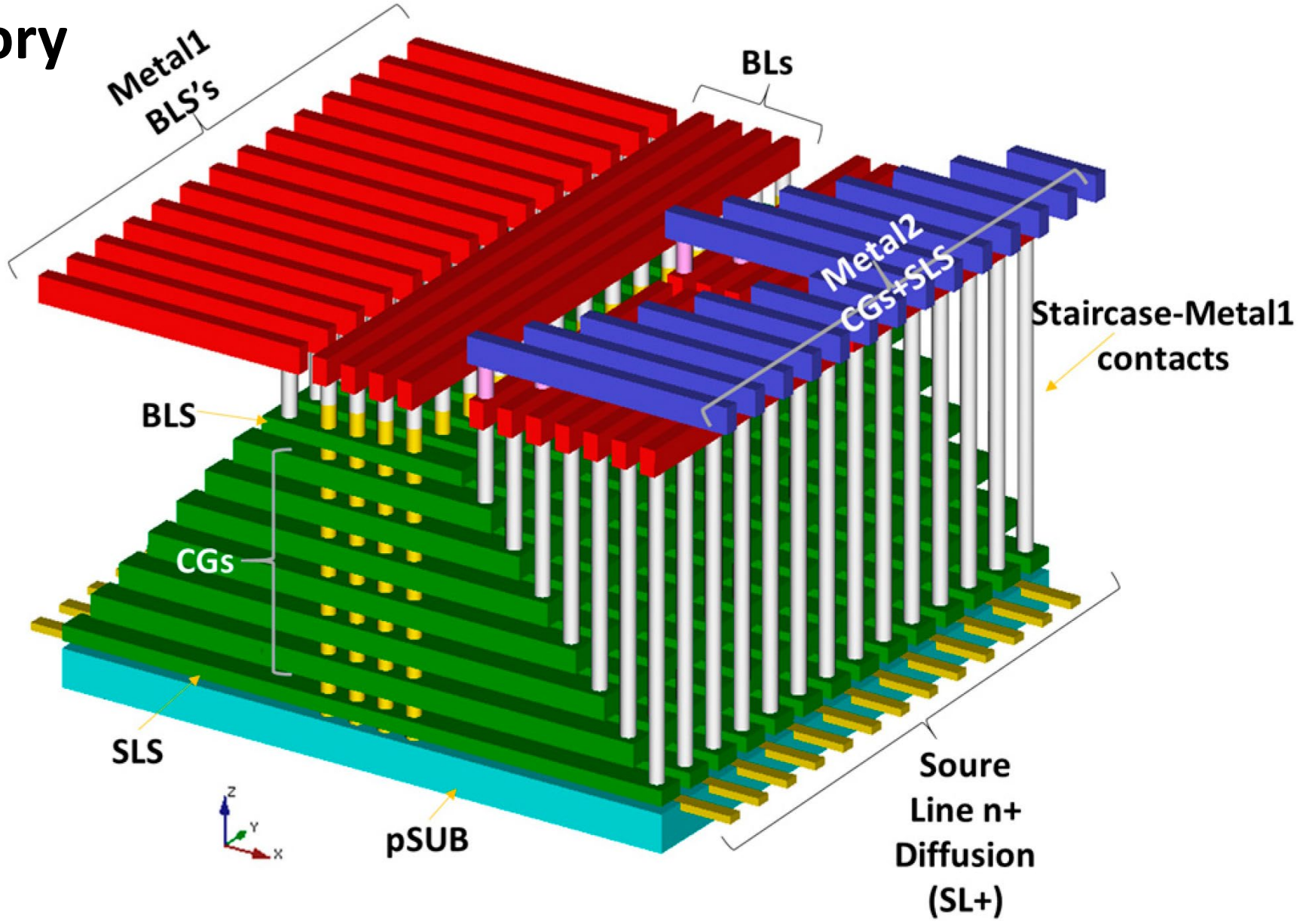
https://semiwiki.com/forum/attachments/4f2-jpg.3294/

https://www.allaboutcircuits.com/uploads/articles/intro_to_DRAM1.png

3D NAND Flash memory

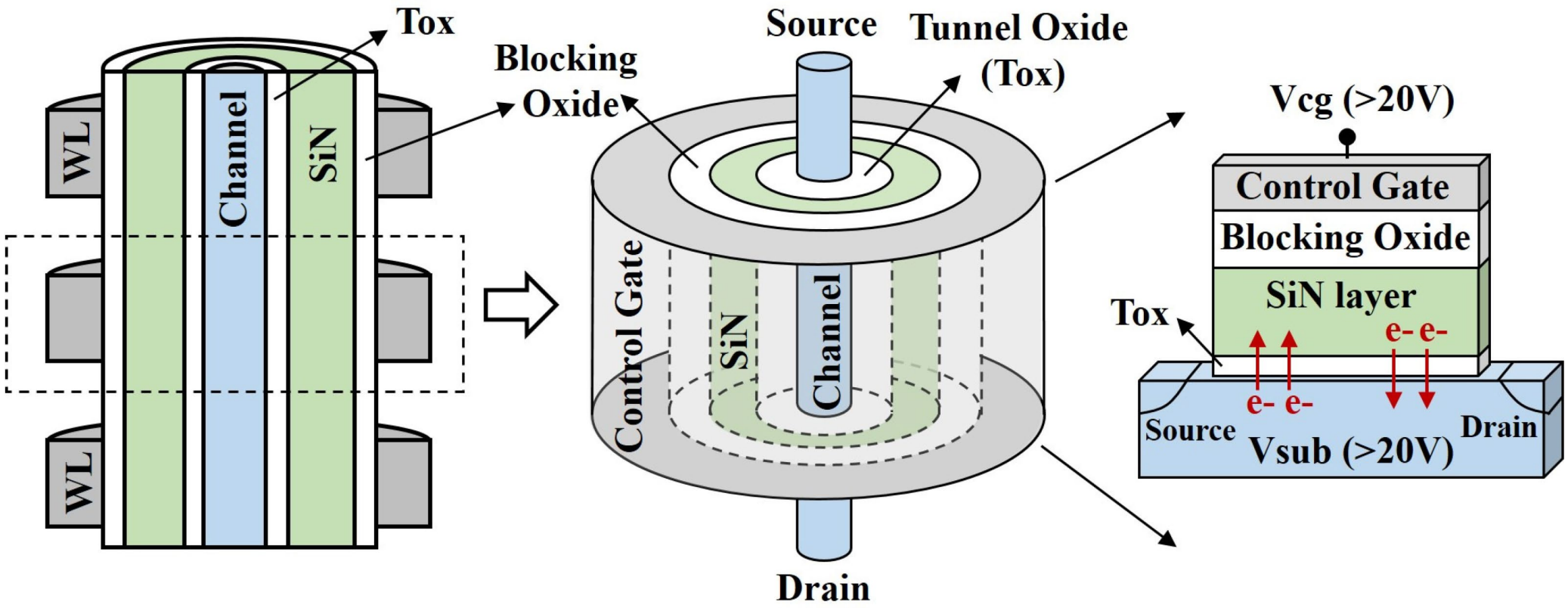
https://dmassets.micron.com/is/image/micronetechnology/nand-flash-worlds-first-layers%3A3-2-all-others?ts=1750894890969&dpr=off

BLS: bit line selector
SLS: source line selector
CG: control gate (word line)
BL: bitline
pSUB: p-type substrate



Micheloni, R. 3D Flash Memories; Springer: Dordrecht, The Netherlands, 2016.

3D NAND Flash memory: memory cell



https://www.mdpi.com/eng/eng-05-00027/article_deploy/html/images/eng-05-00027-g004.png

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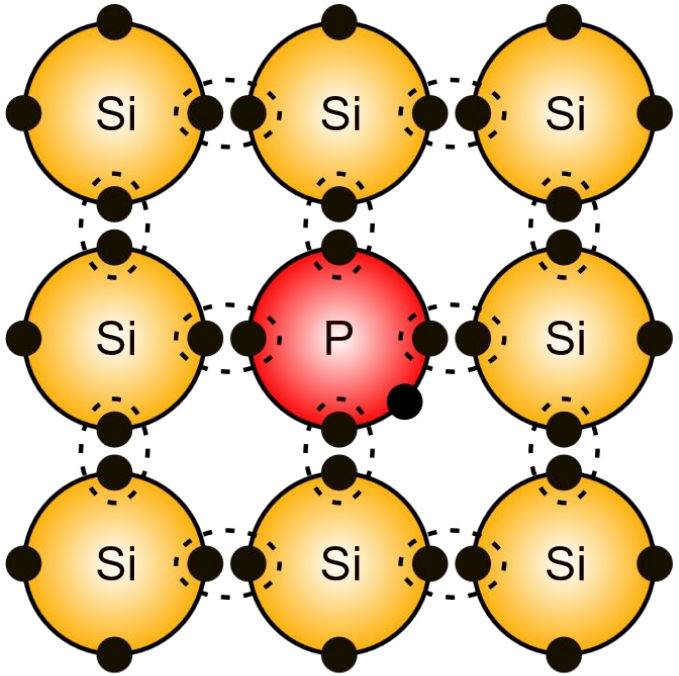
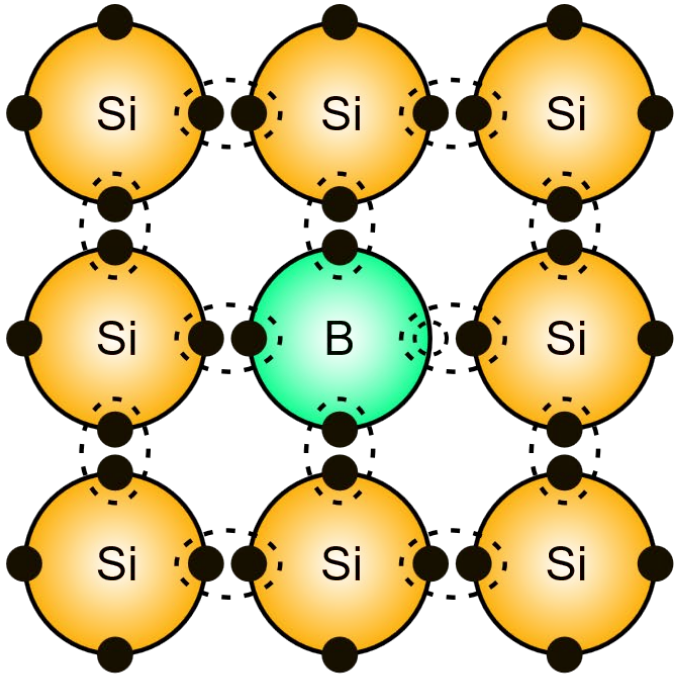


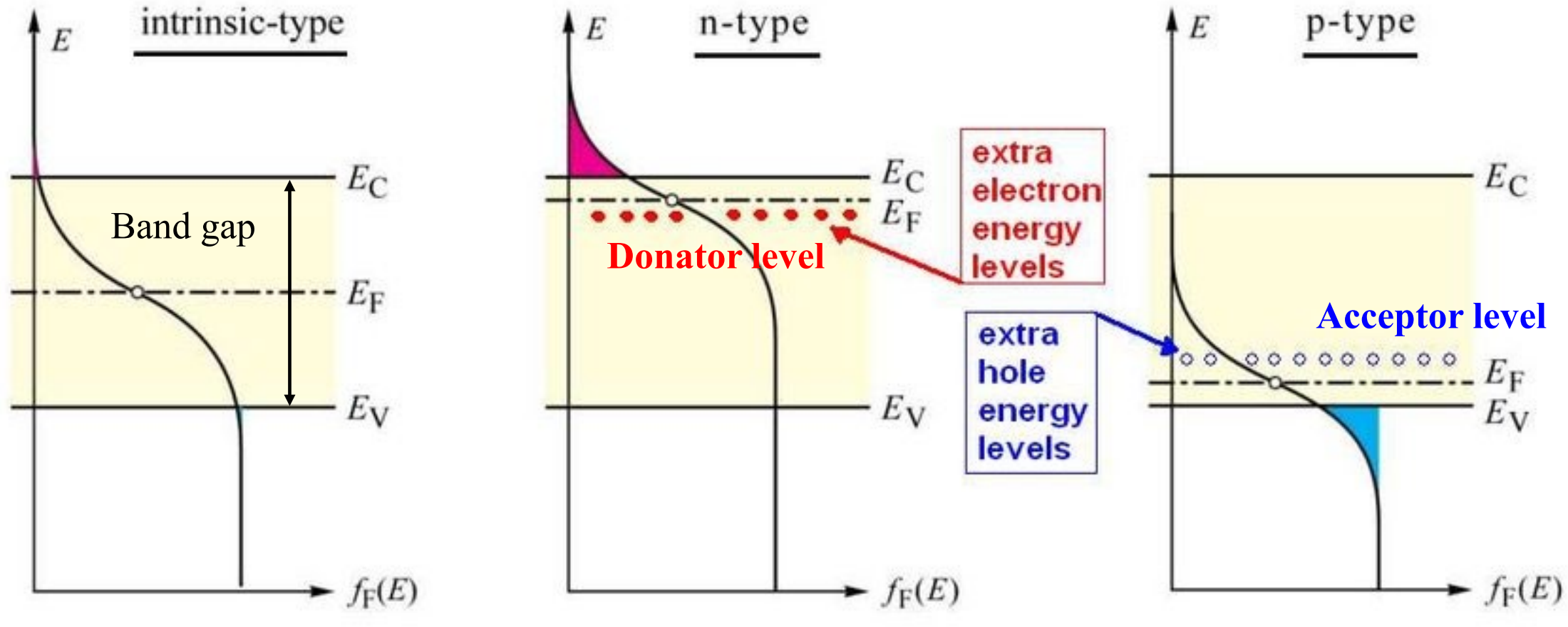
n-type



p-type

https://devxplained.eu/user/pages/02.blog/p-n-junction/silicon-doping.svg?decoding=auto&fetchpriority=auto&g-982d5237

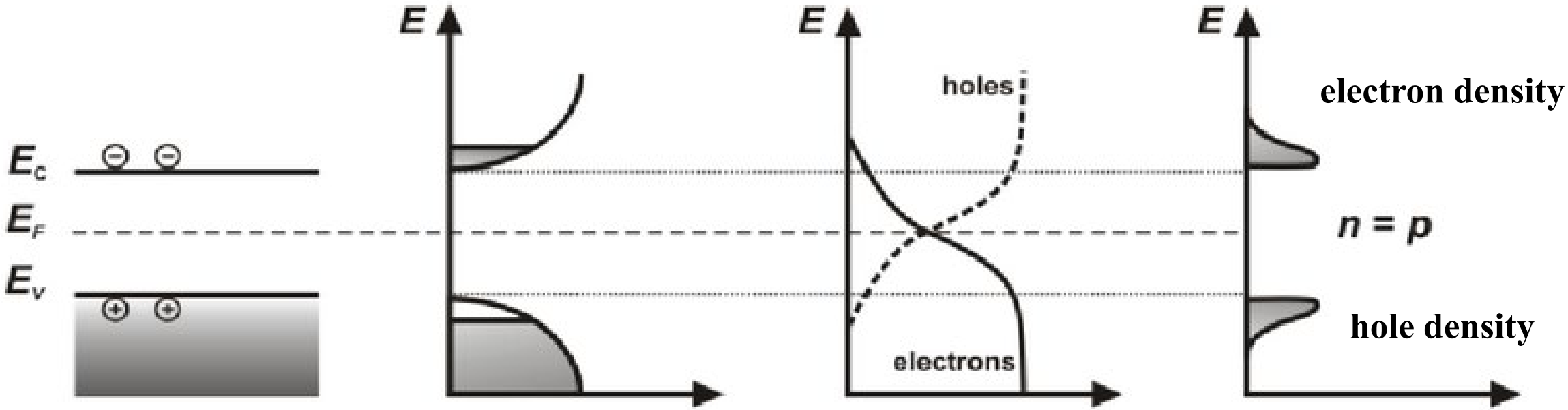
$f_F(E)$: Fermi-Dirac distribution function



E_c: conduction band energy, E_F: Fermi energy, E_V: Valence band energy

https://i.sstatic.net/72aOy.jpg

For Intrinsic Si (i.e., without dopants)

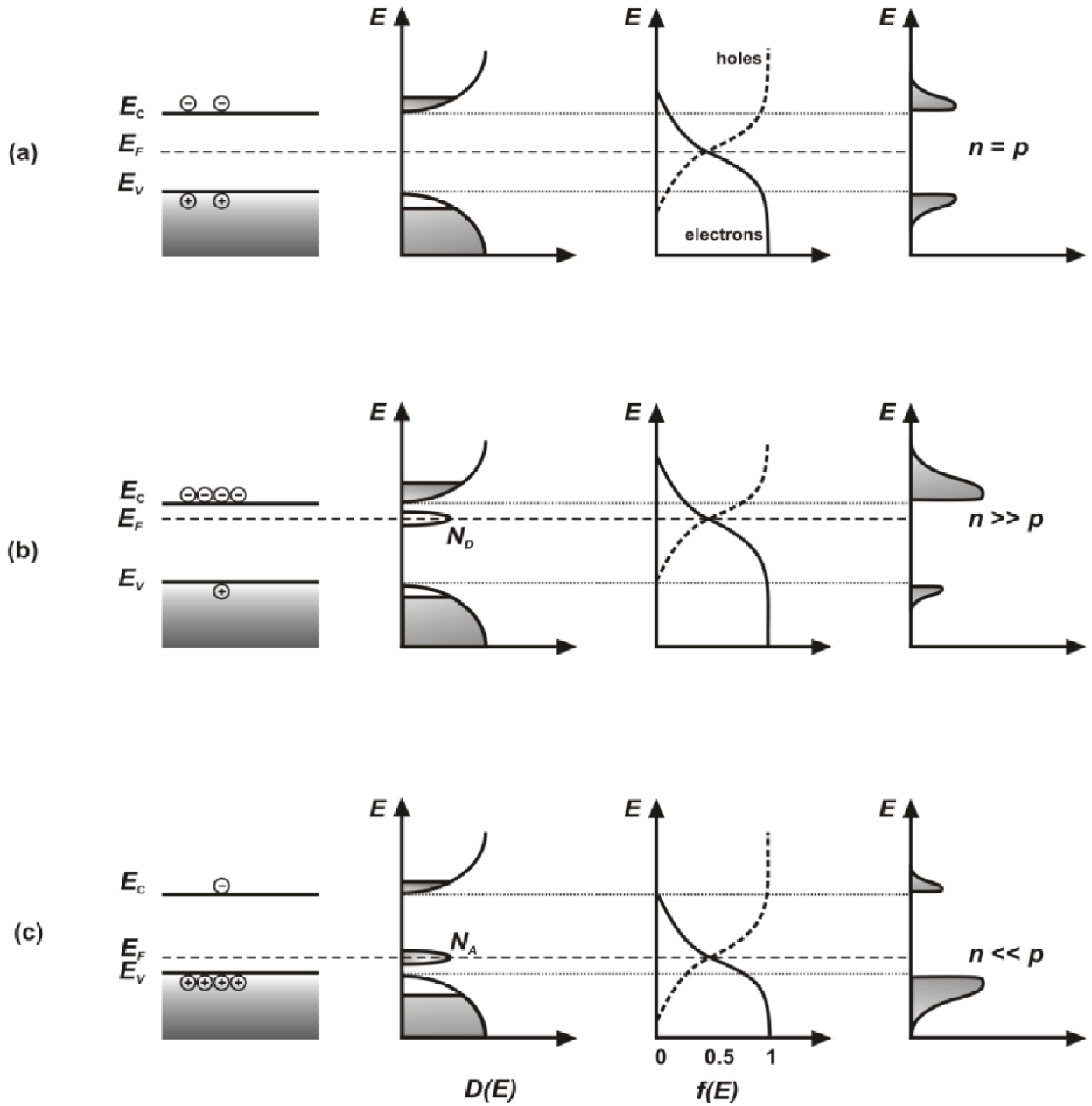


Density of states (DOS)

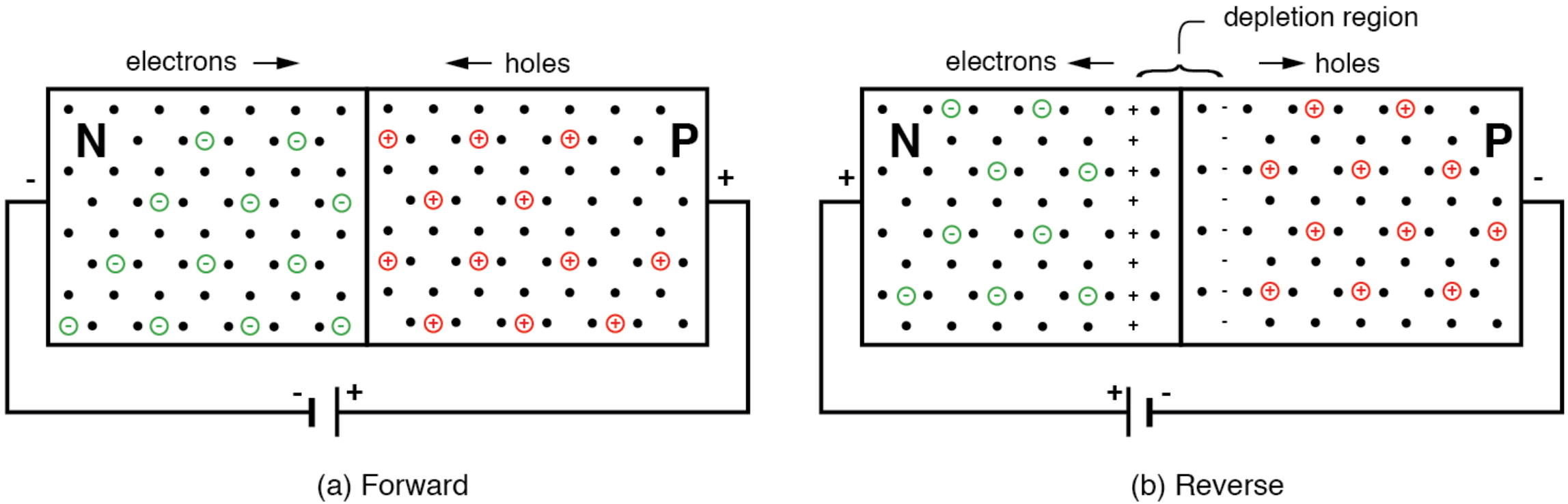
Fermi-Dirac function

Carrier densities

https://i.sstatic.net/k5RID.png

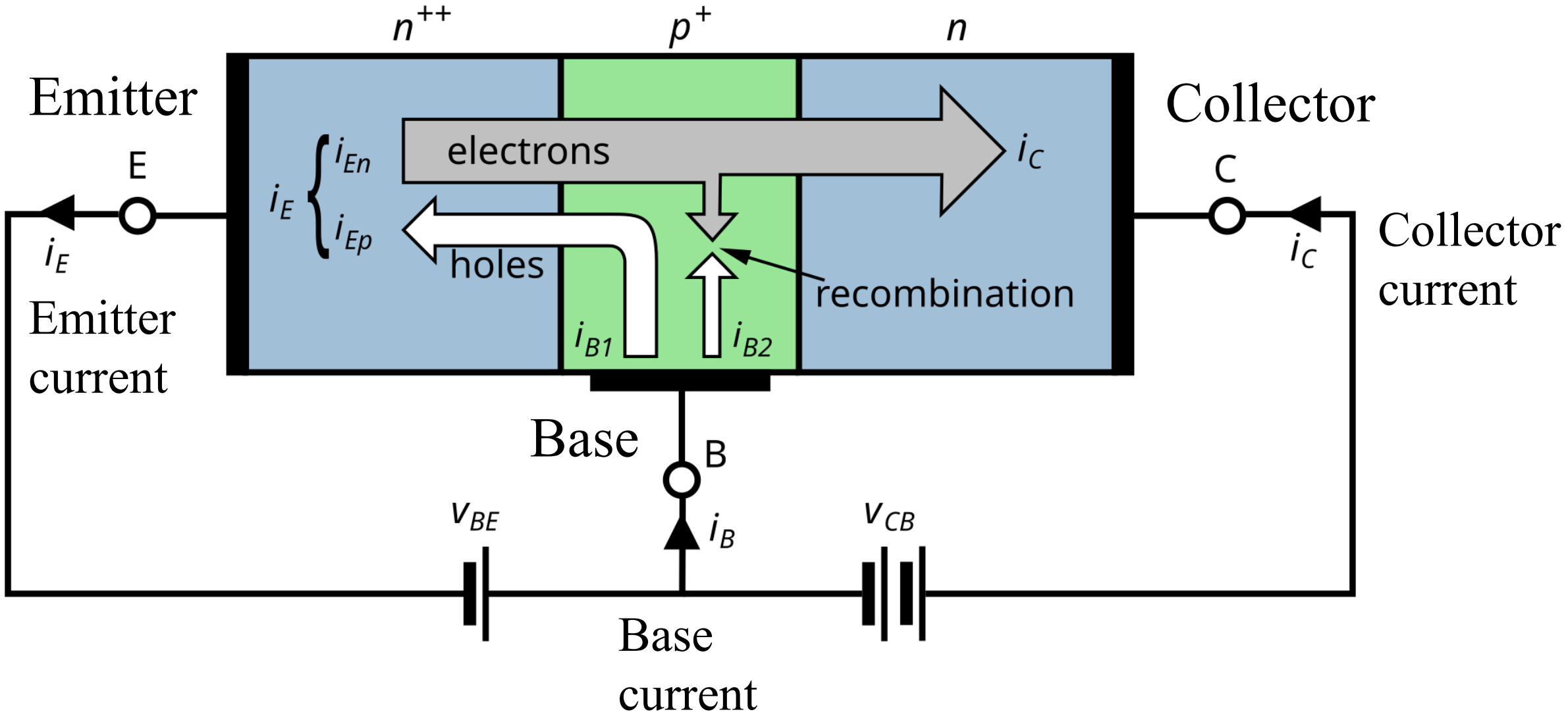

(a)
E
E
E
holes
E_c
E_F
E_v
electrons
n = p
(b)
E
E
E
E_c
E_F
N_D
E_v
n >> p
(c)
E
E
E
E_c
E_F
E_v
N_A
n << p
0
0.5
1
D(E)
f(E)

PN junction diode



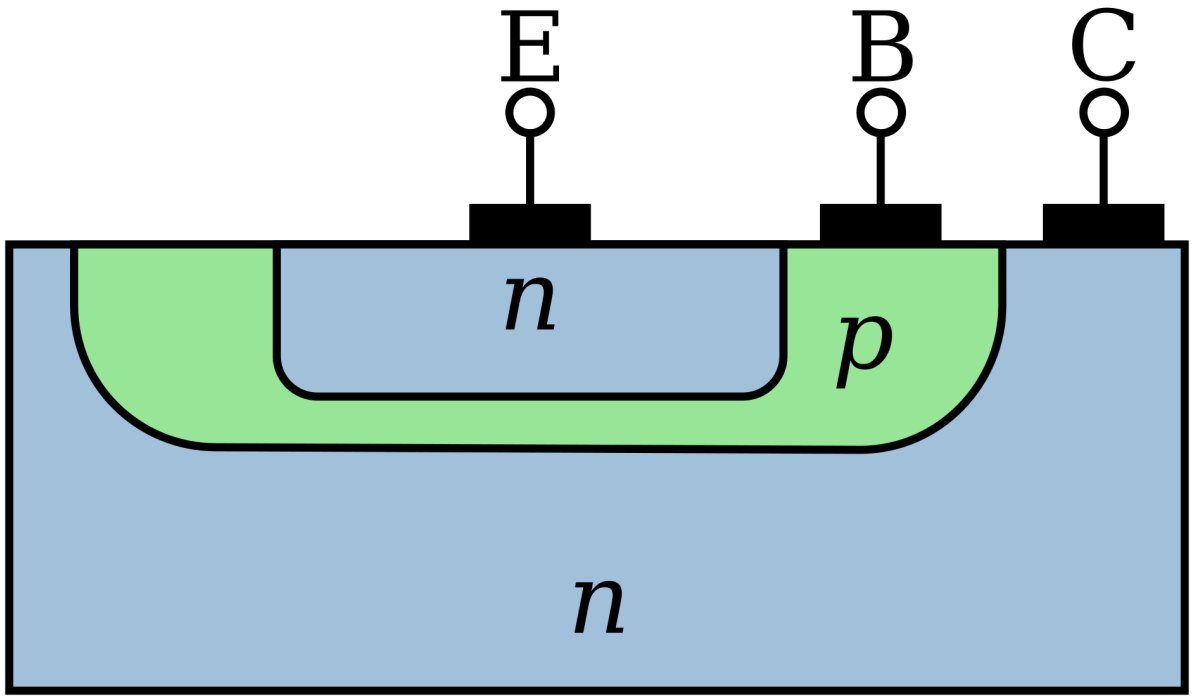
https://www.allaboutcircuits.com/uploads/articles/pn-junction-bias.png

Bipolar Junction Transistor (BJT) : NPN transistor



https://en.wikipedia.org/wiki/Bipolar_junction_transistor

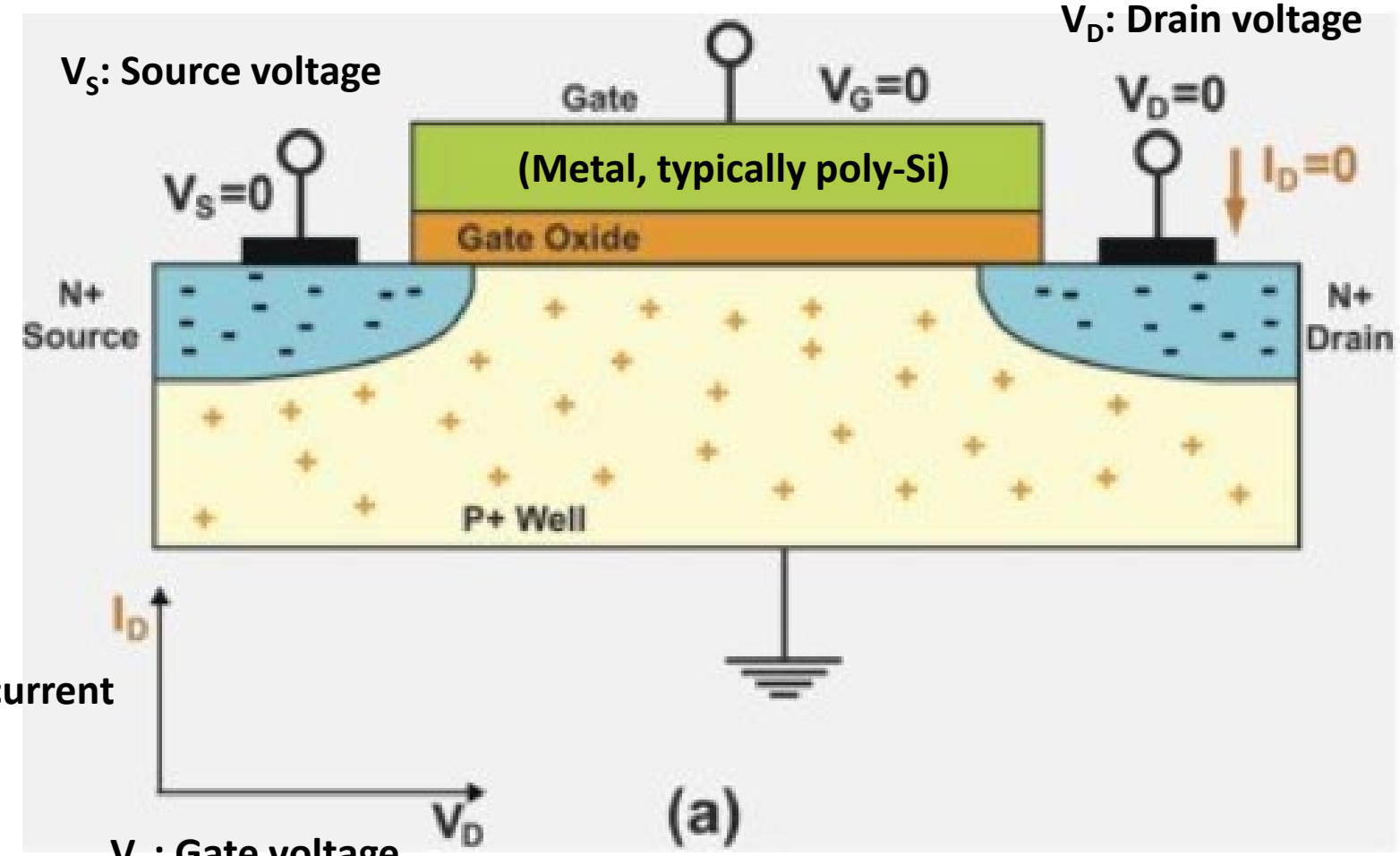
Bipolar Junction Transistor (BJT) : NPN transistor



Simplified cross section of a planar *NPN* bipolar junction transistor

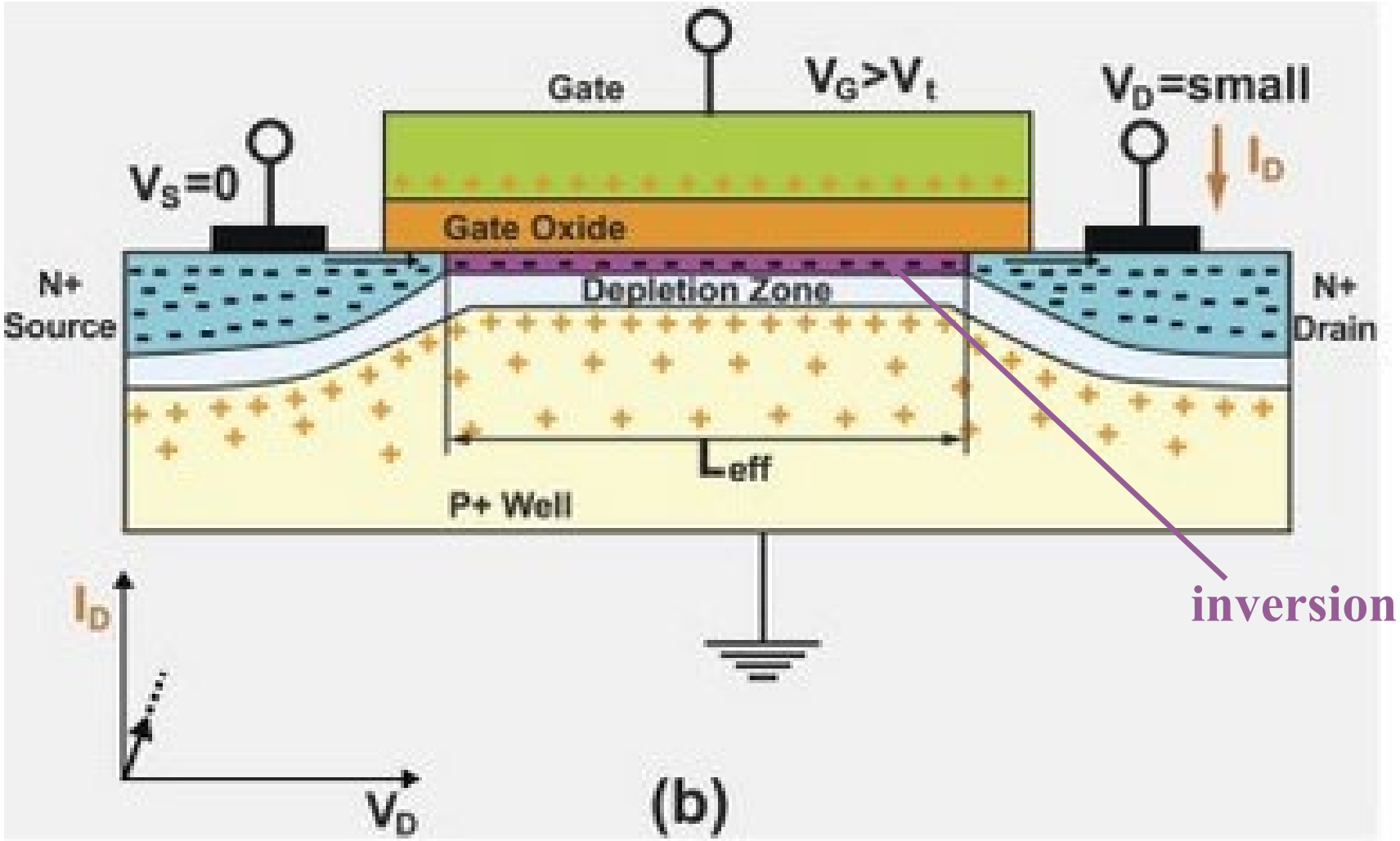
https://en.wikipedia.org/wiki/Bipolar_junction_transistor

Metal–Oxide–Semiconductor Field-Effect Transistor (MOS FET)



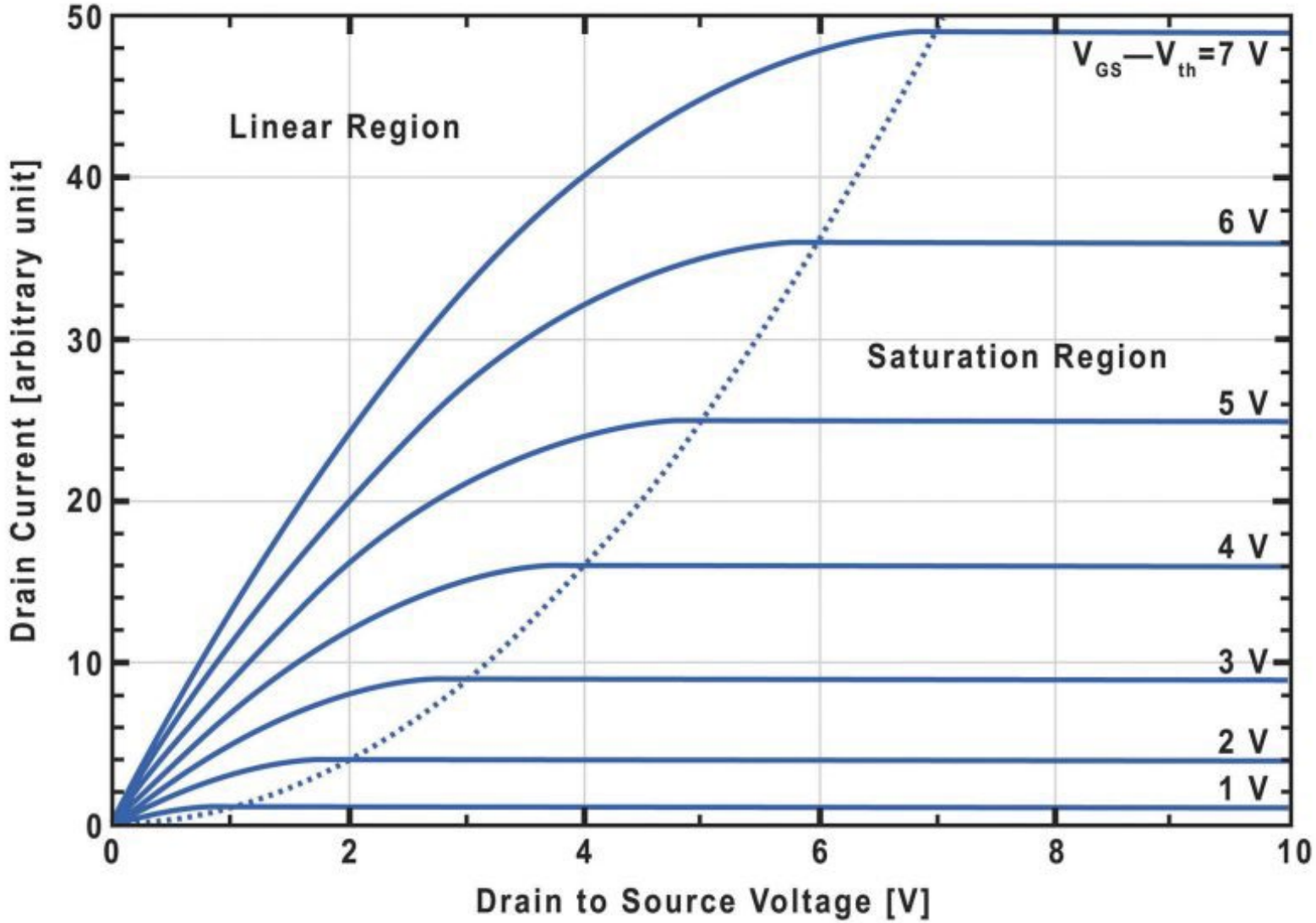
https://www.mks.com/n/mosfet-physics

Metal–Oxide–Semiconductor Field-Effect Transistor (MOS FET)



https://www.mks.com/n/mosfet-physics

V_{GS}: gate voltage – source voltage V_{th}: Threshold voltage



https://www.mks.com/n/mosfet-physics

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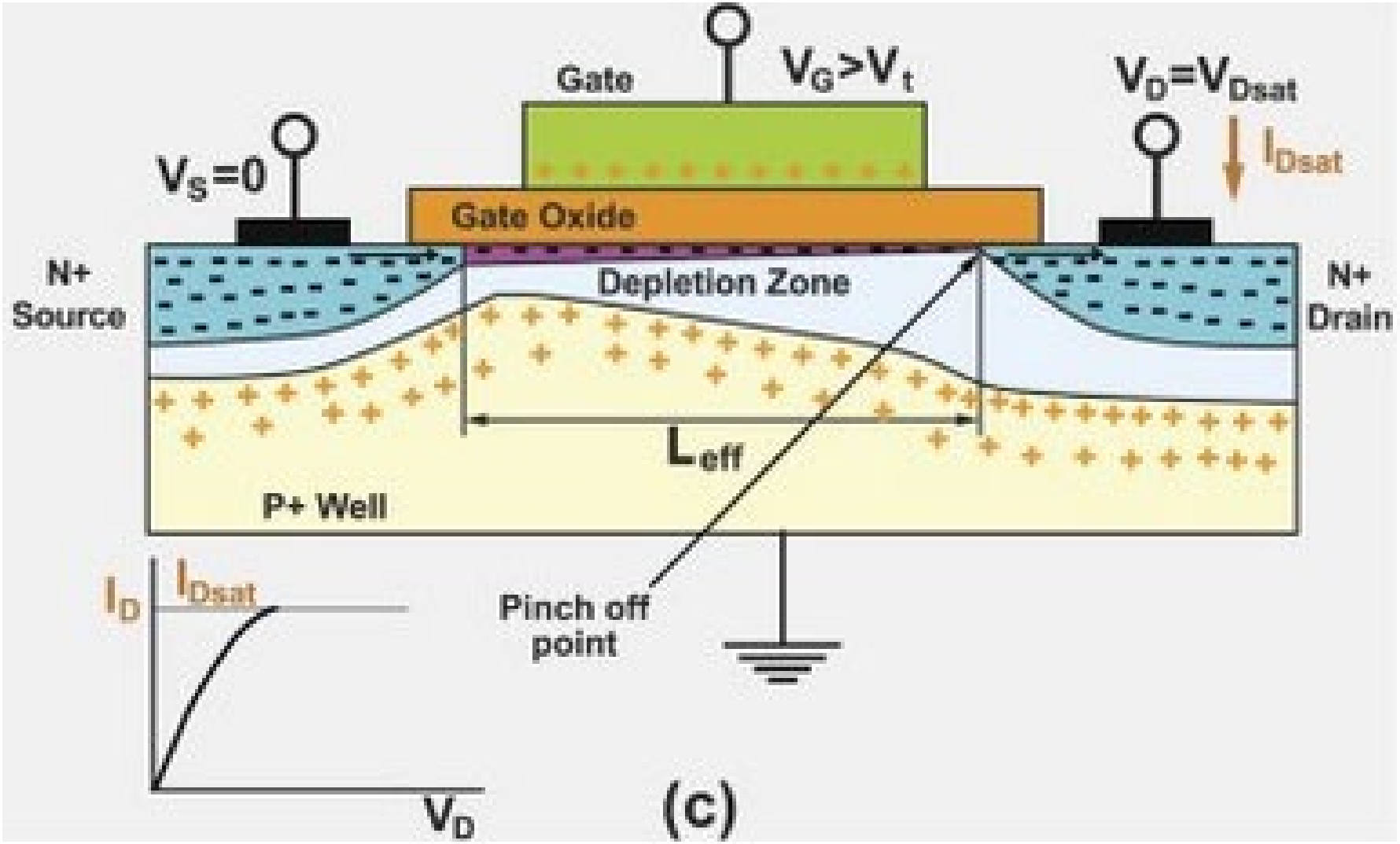
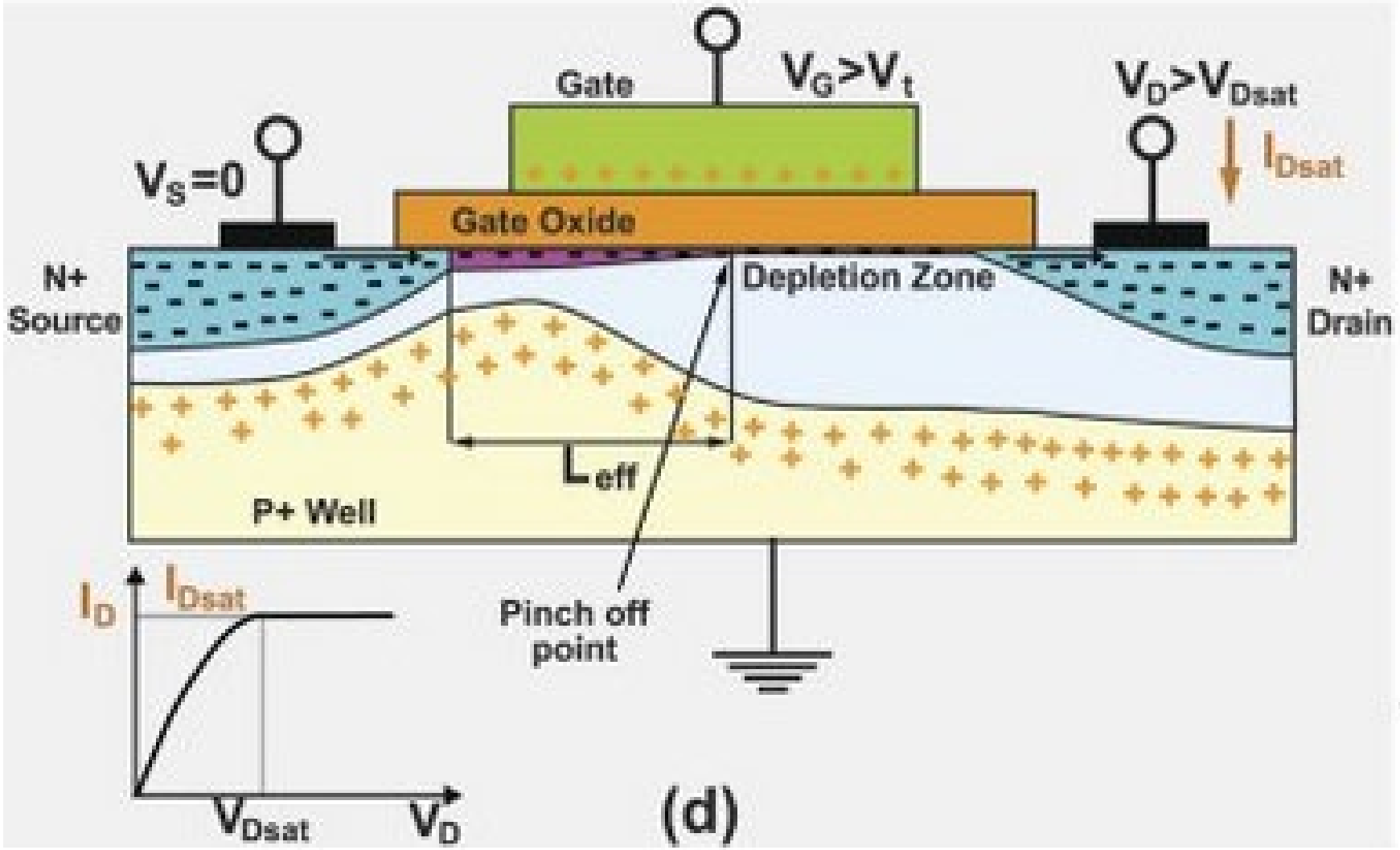
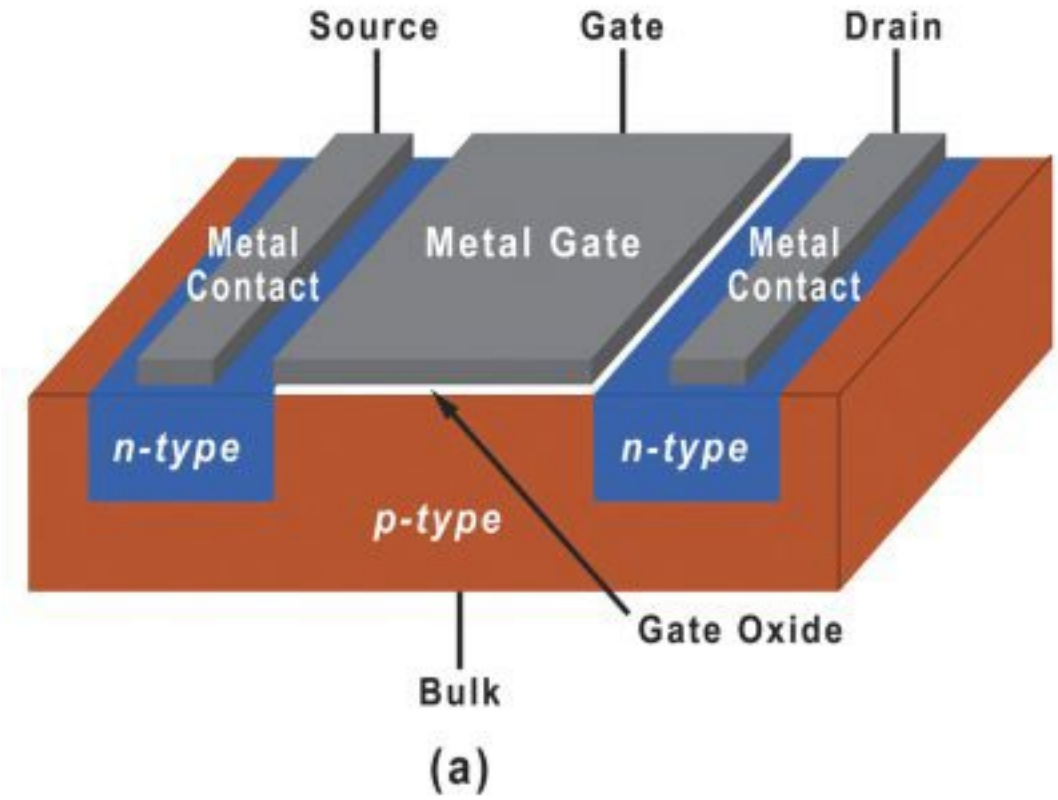


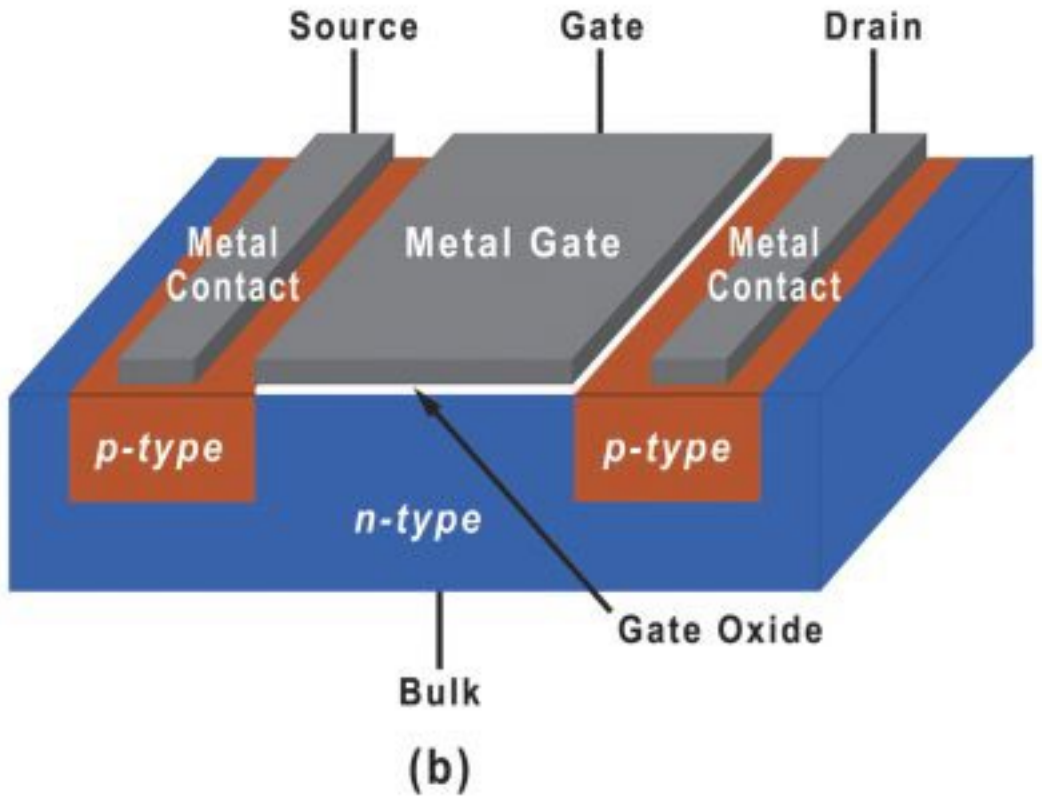
Metal–Oxide–Semiconductor Field-Effect Transistor (MOS FET)



NMOS

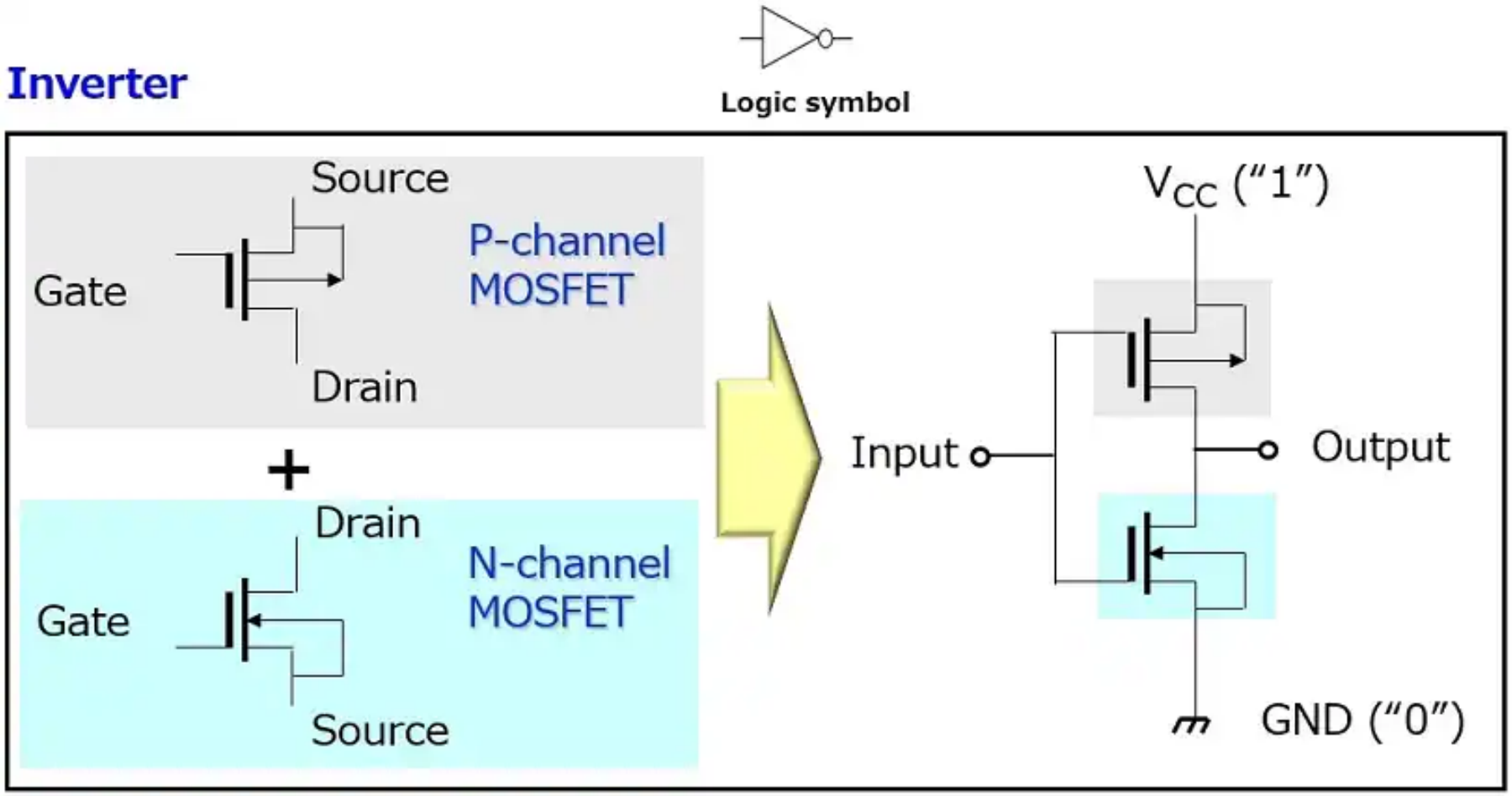


PMOS



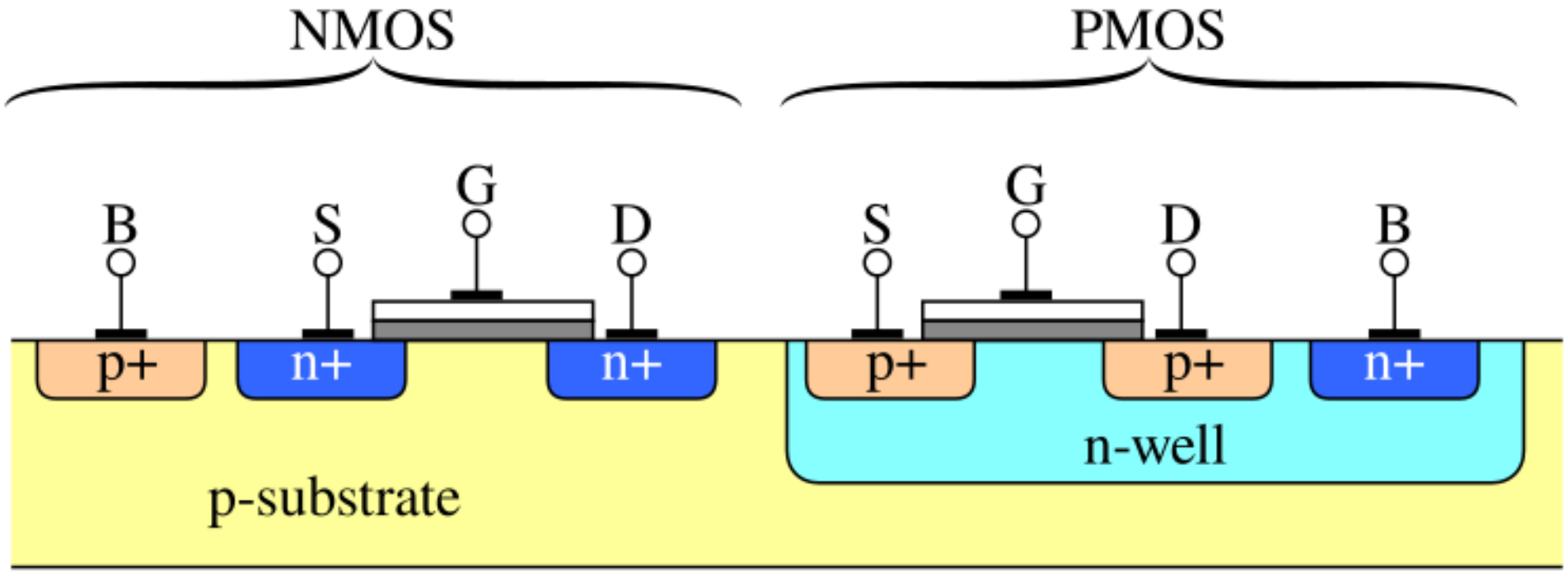
MOS consumes much less power than BJT

Complementary MOS FET (CMOS)



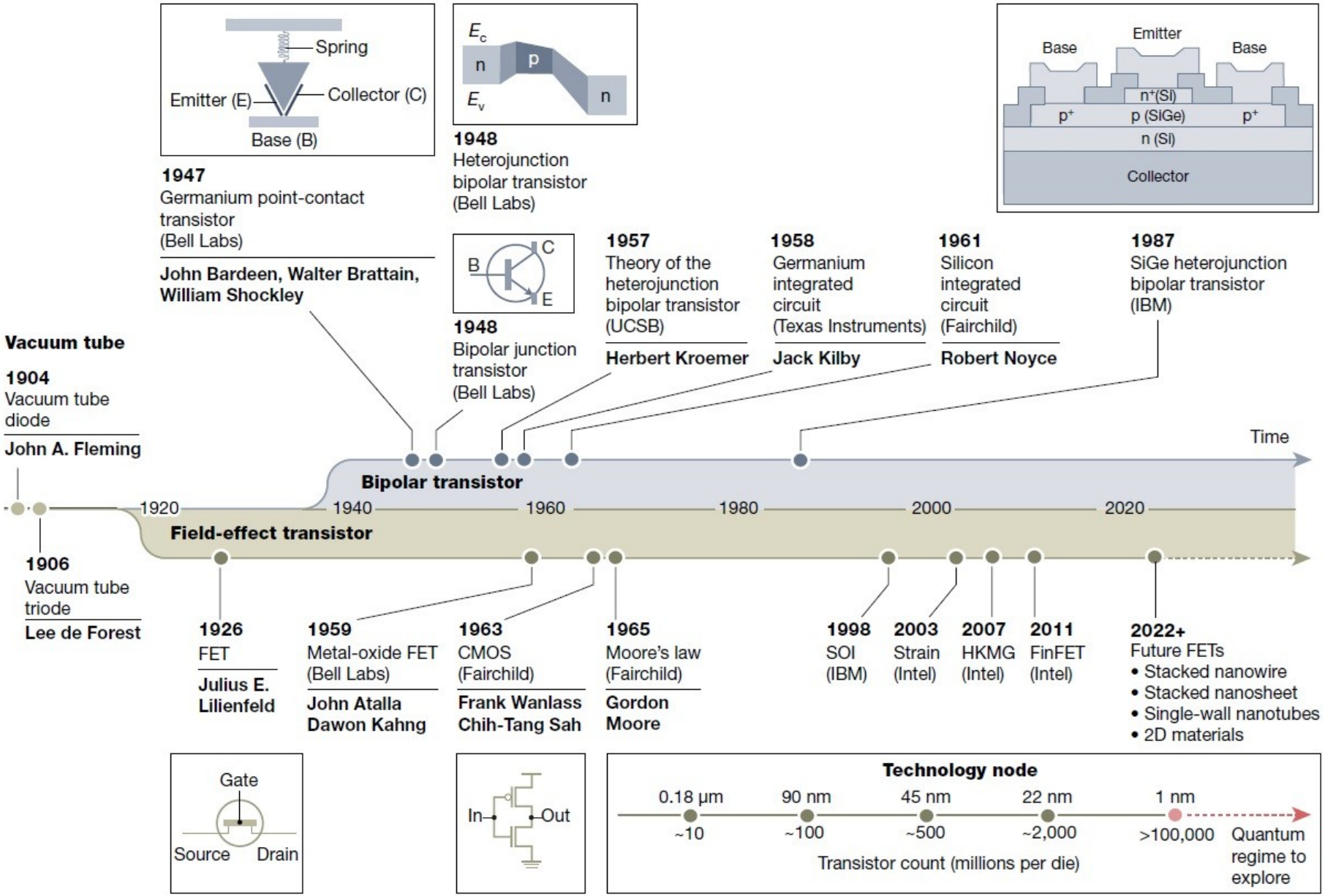
https://toshiba.semicon-storage.com/content/dam/toshiba-ss-v3/master/en/semiconductor/knowledge/e-learning/cmos-logic-basics/chap2-1_en.jpg

Complementary MOS FET (CMOS)



D: Drain
S: Source
G: Gate
B: Bulk

The advantages of CMOS over NMOS or PMOS are
lower power consumption, less prone to noise, and therefore, allow higher integration.



(patent only)

https://media.licdn.com/dms/image/v2/D4E12AQGdKSE-jbRPTQ/article-cover_image-shrink_720_1280/article-cover_image-shrink_720_1280/0/1735757501914?e=1759363200&v=beta&t=1bVY24kkGDq3UzxitG3KiPtZtEPaM0b5Y7cN8O0wqvo

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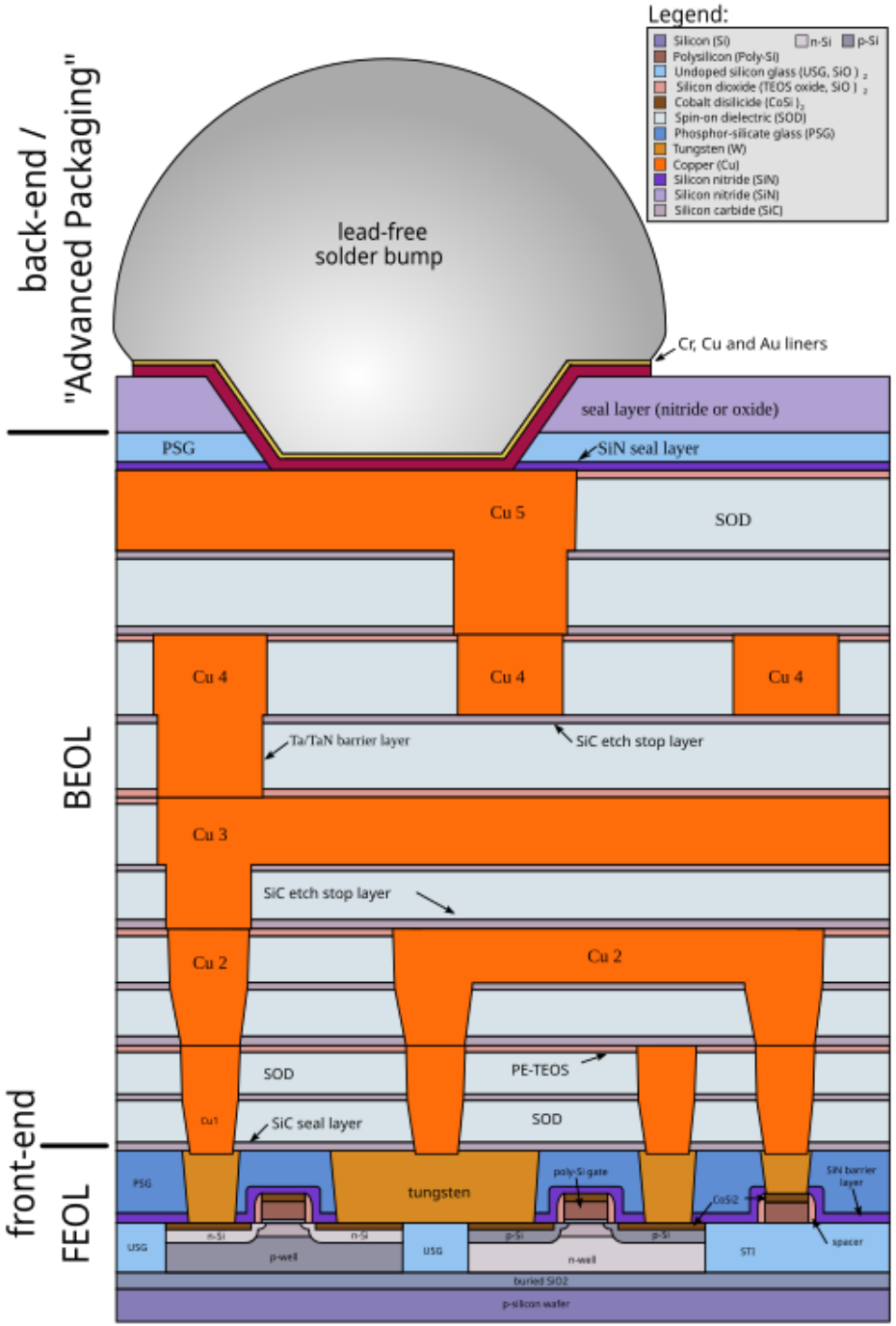
Outline of semiconductor manufacturing

Cross-section of a chip ⇒

- **front-end processes**
  - **front end of line (FEOL)**
  - **back end of line (BEOL)**
- **back-end processes**



https://upload.wikimedia.org/wikipedia/commons/thumb/e/ee/Cmos-chip_structure_in_2000s_%28en%29.svg/500px-Cmos-chip_structure_in_2000s_%28en%29.svg.png

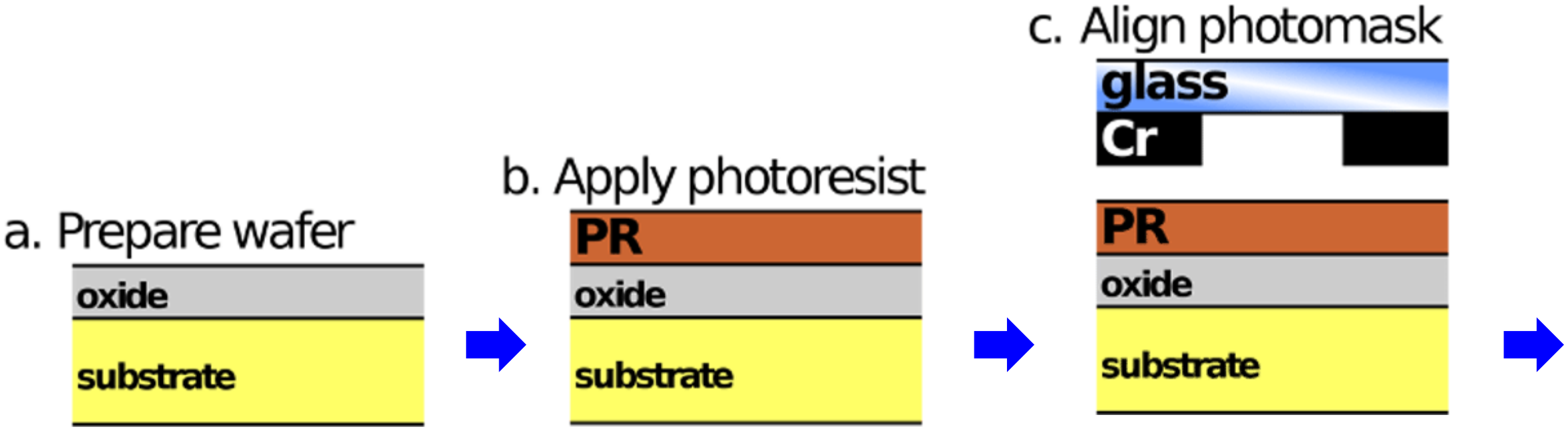
FOEL processes

FEOL processes: the first portion of IC fabrication where the individual components (transistors, capacitors, resistors, etc.) are patterned in a semiconductor substrate. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers.

(https://en.wikipedia.org/wiki/Front_end_of_line)

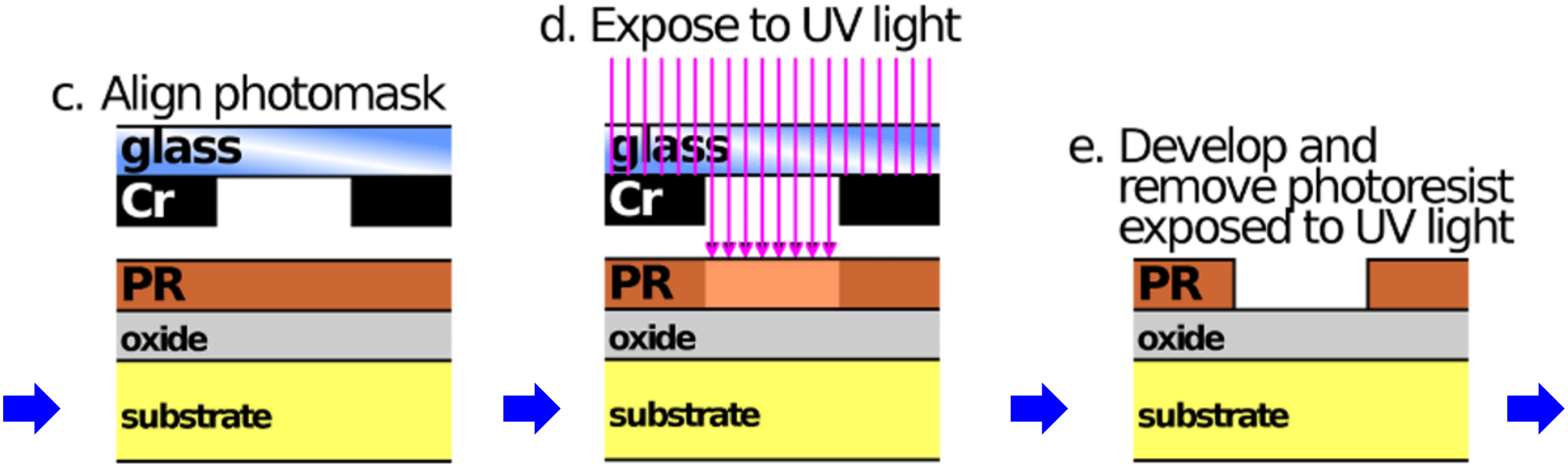
Basic Pattern Formation Process

How to form a mask for plasma etching



Basic Pattern Formation Process

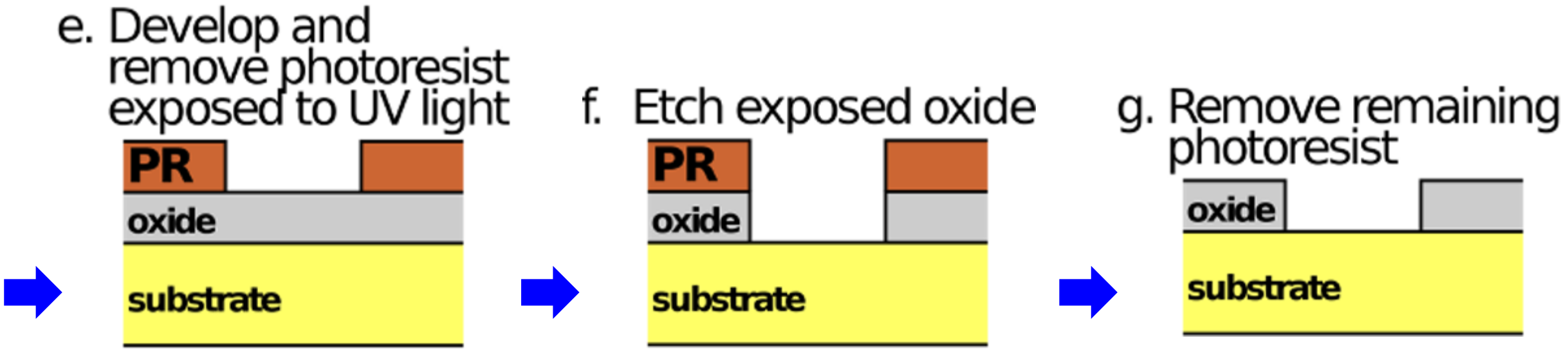
How to form a mask for plasma etching



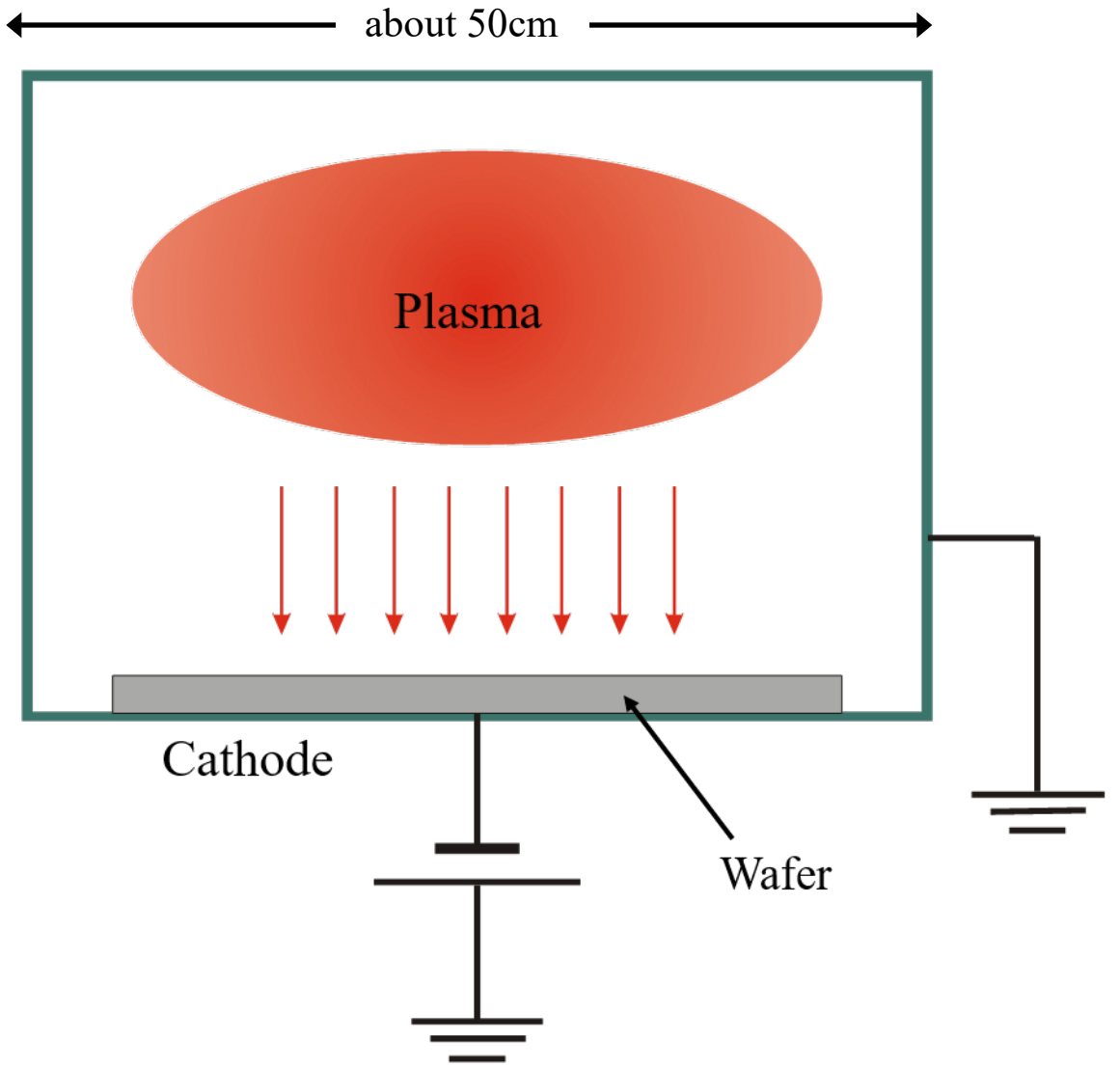
Lithography process

Basic Pattern Formation Process

How to form a mask for plasma etching

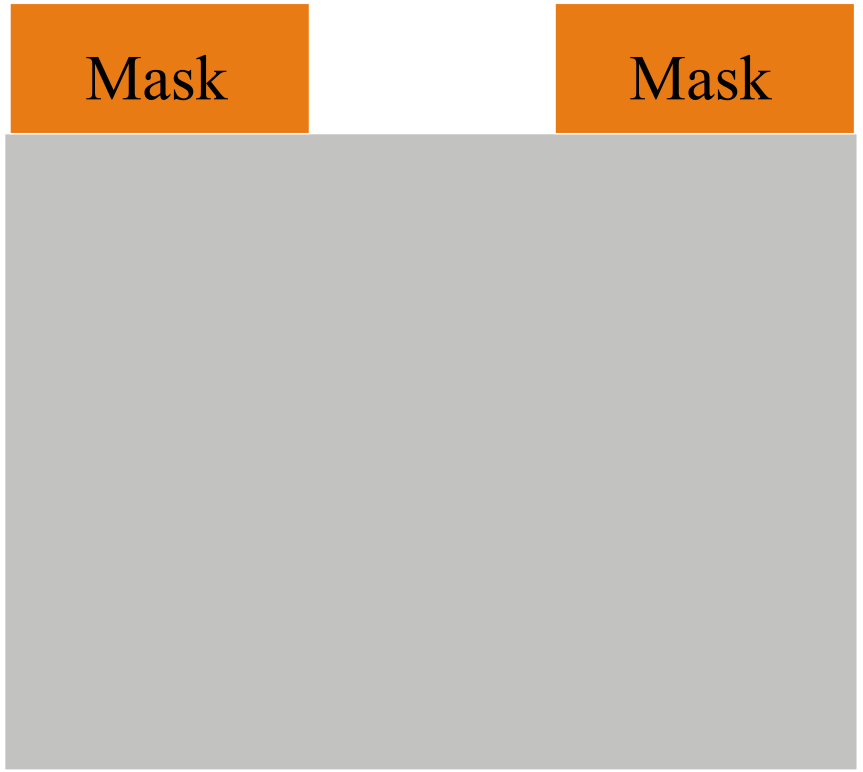


Typical Plasma Processing Equipment

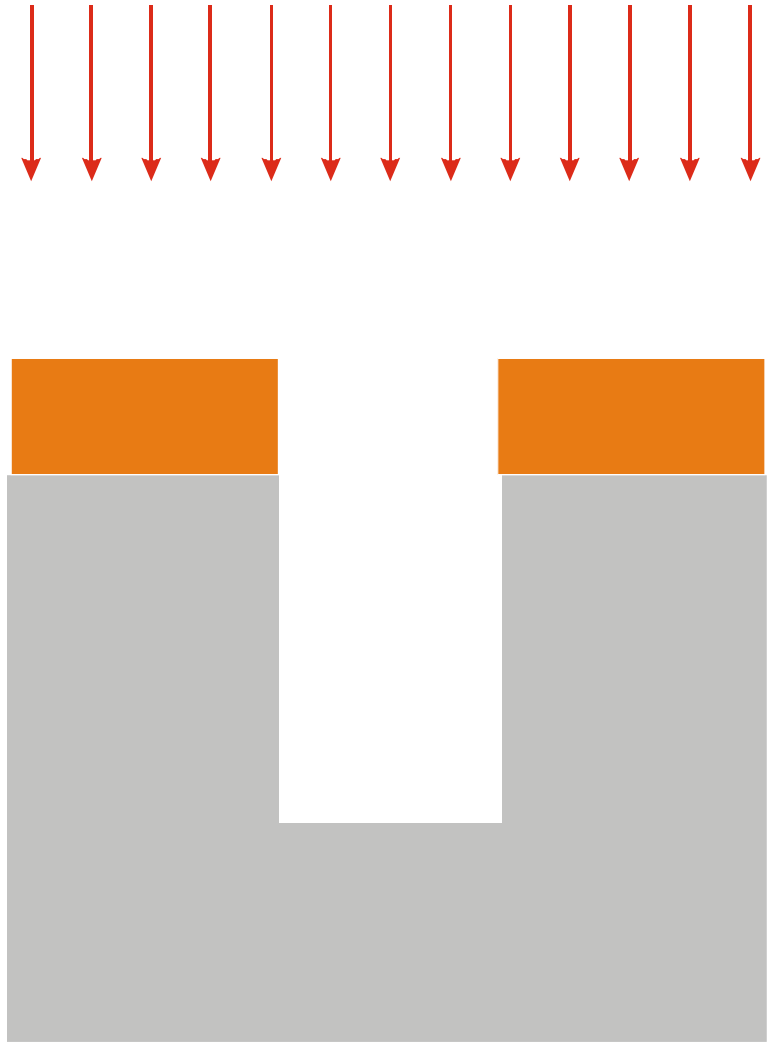


Chip Surface

For example, about 100 nm

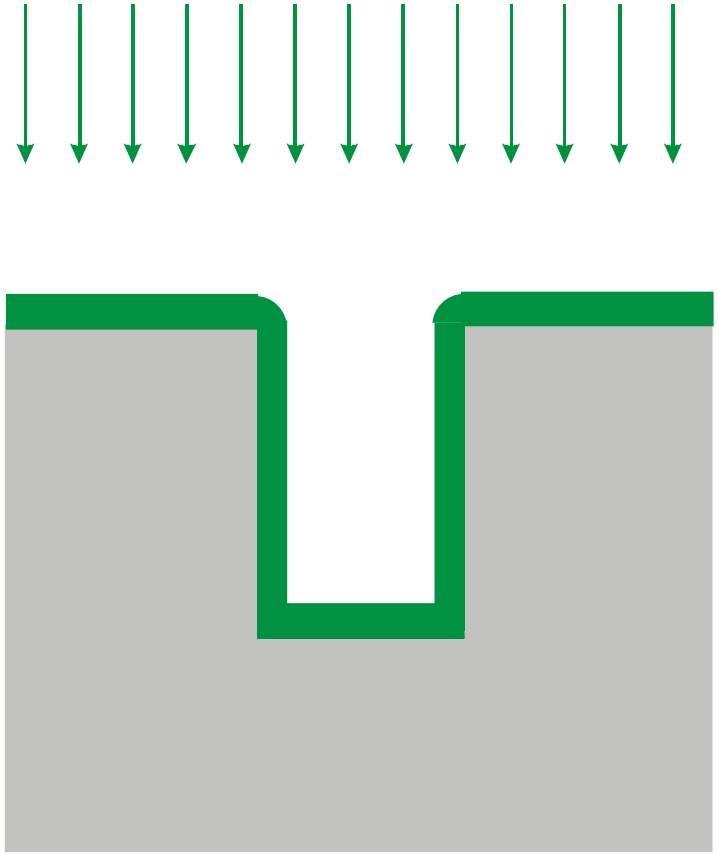


Dig a hole or Trench



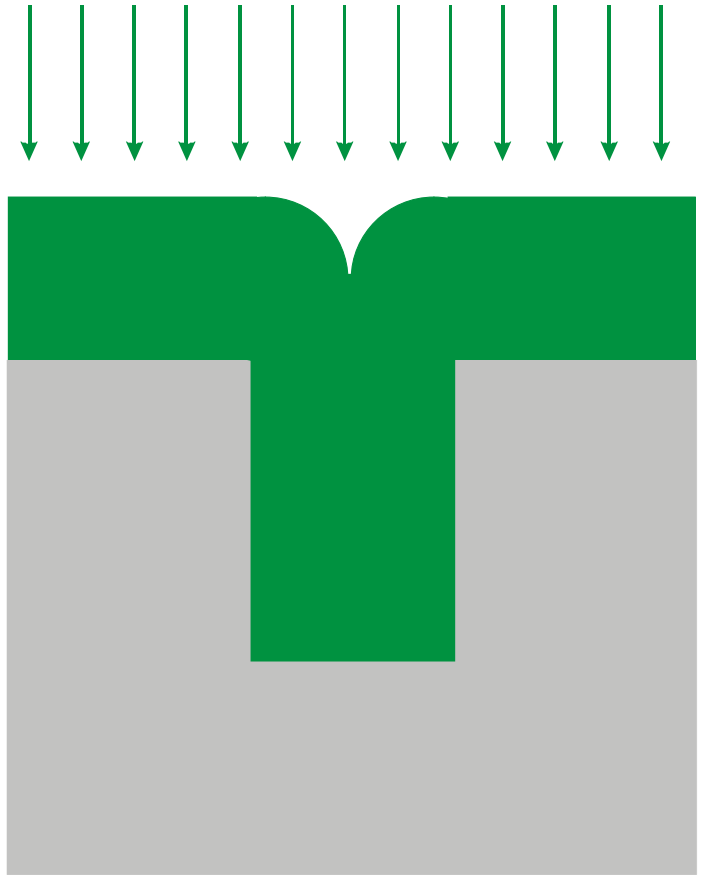
Remove the masks

Fill the Hole or Trench

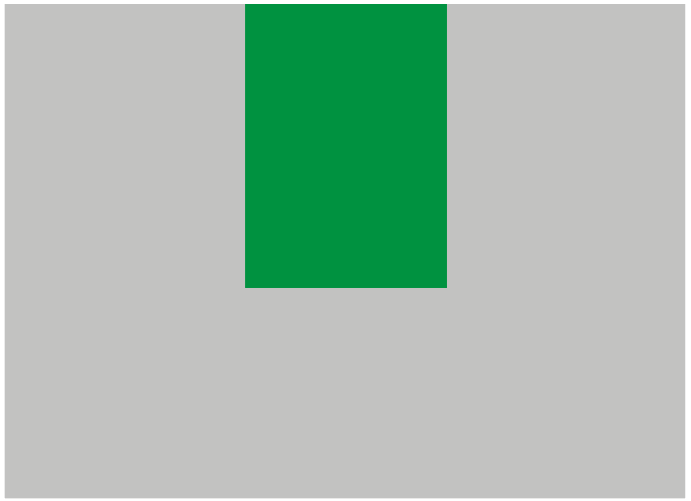


by Chemical Vapor Deposition (CVD)
or Sputtering Deposition (Physical Vapor Deposition: PVD)

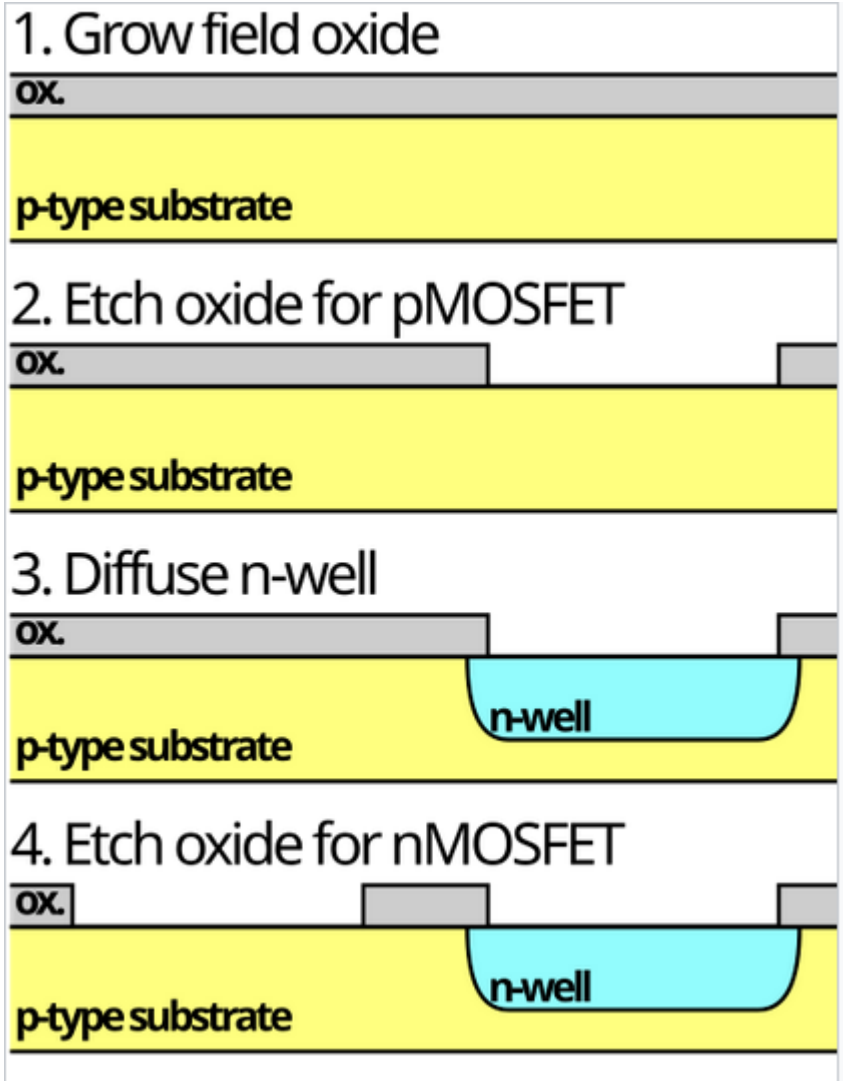
Fill the Hole or Trench



Planarize by Chemical Mechanical Polish (CMP)

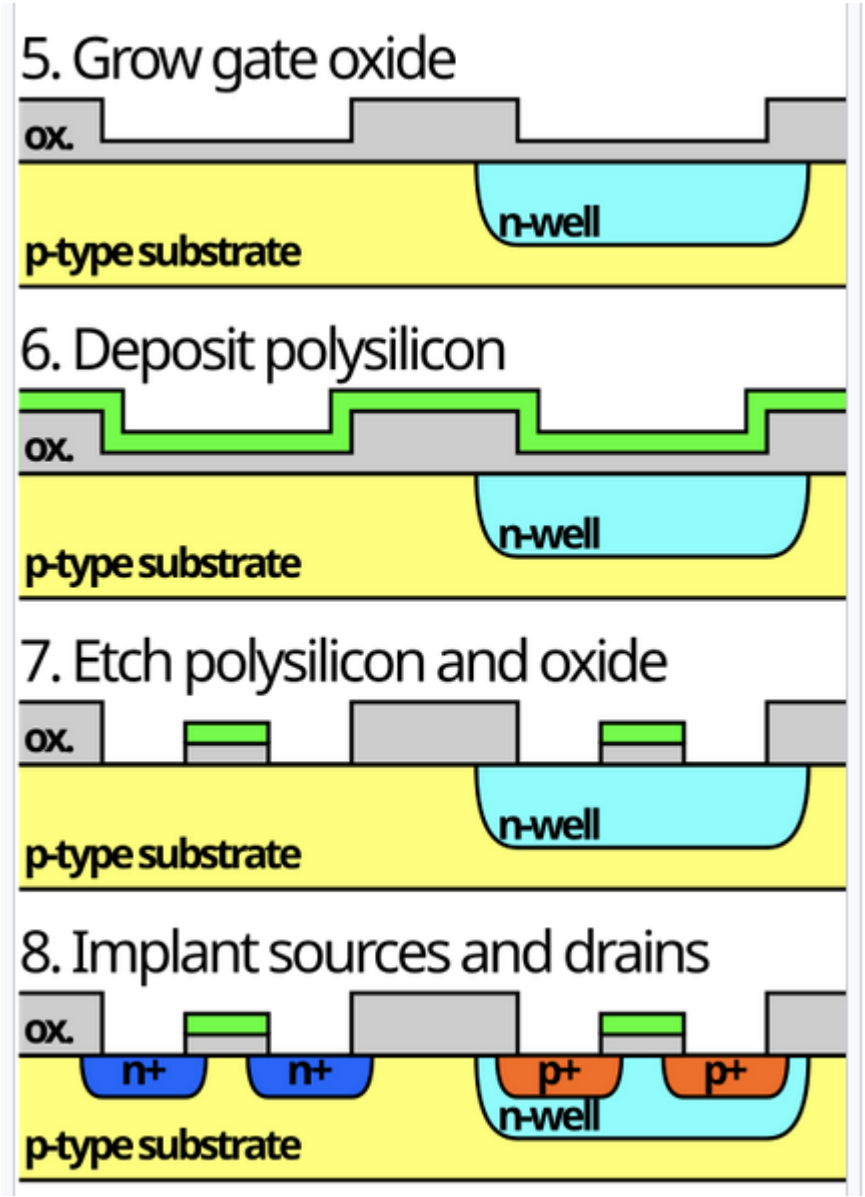


Typical CMOS fabrication process



⇐ **ion implantation**

https://en.wikipedia.org/wiki/Front_end_of_line



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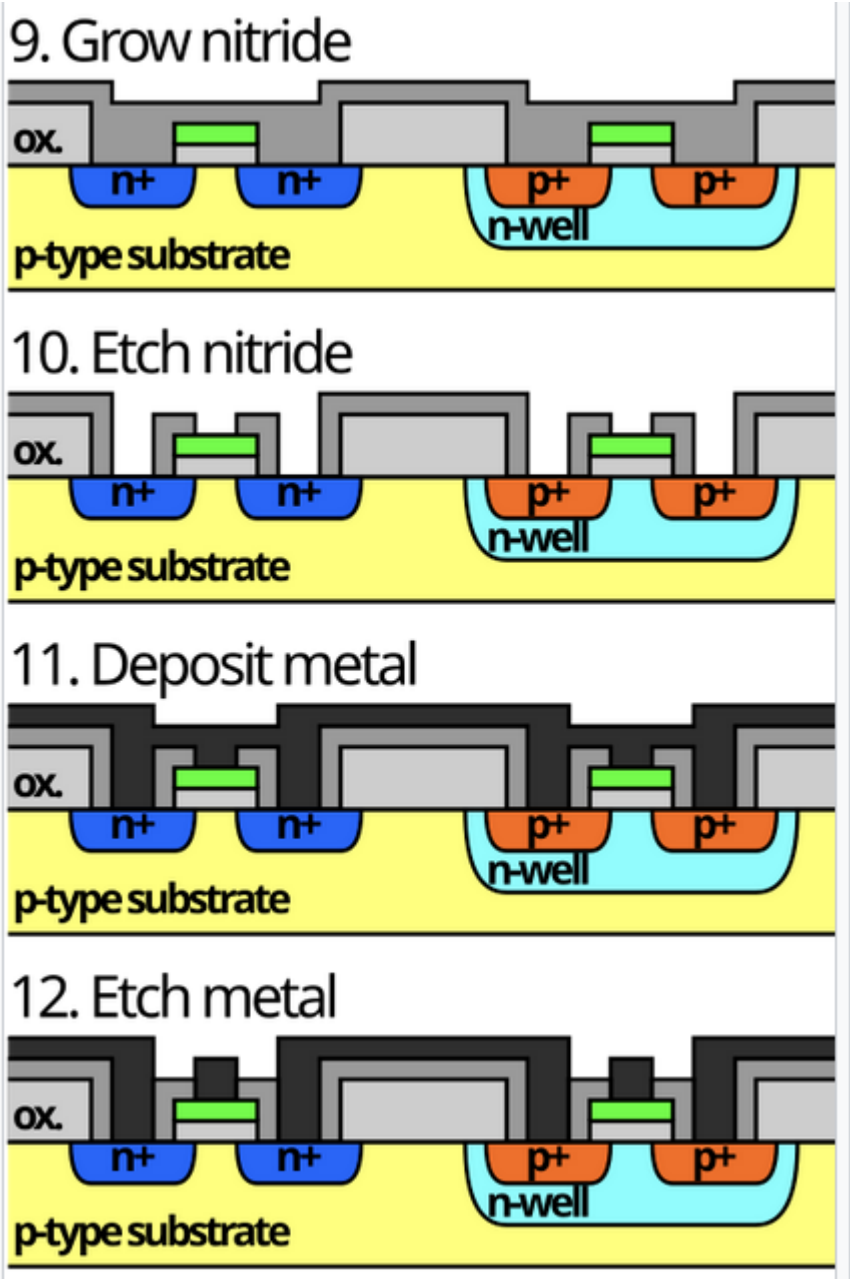


⇐ W deposition: CVD
(for higher layers, Cu is used via electrochemical deposition; damascene process)

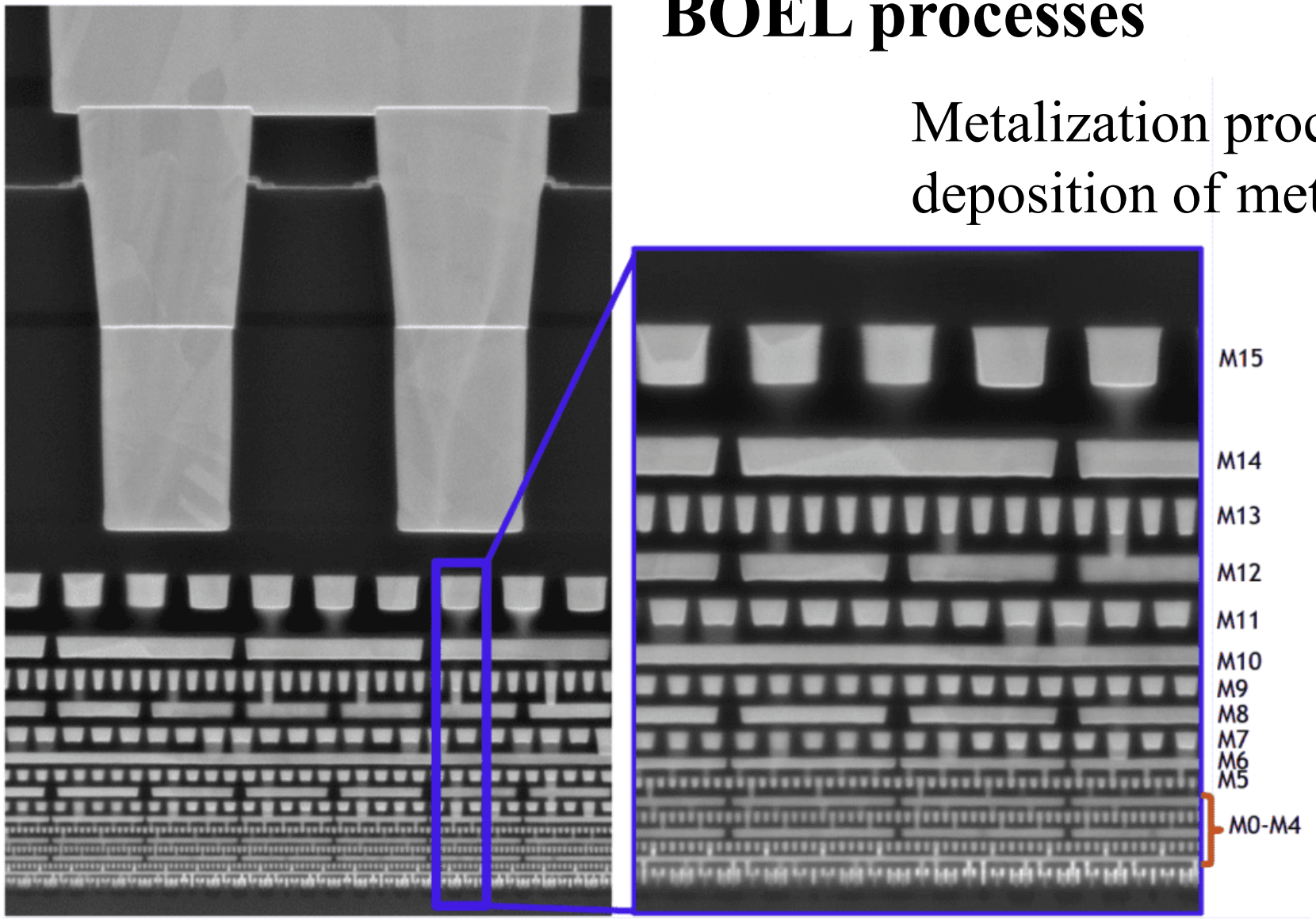
BOEL processes

BEOL processes: the process in semiconductor device fabrication that consists of depositing metal interconnect layers onto a wafer already patterned with devices. It is the second part of IC fabrication, after FEOL. In BEOL, the individual devices (transistors, capacitors, resistors, etc.) are connected to each other according to how the metal wiring is deposited. (https://en.wikipedia.org/wiki/Back_end_of_line)

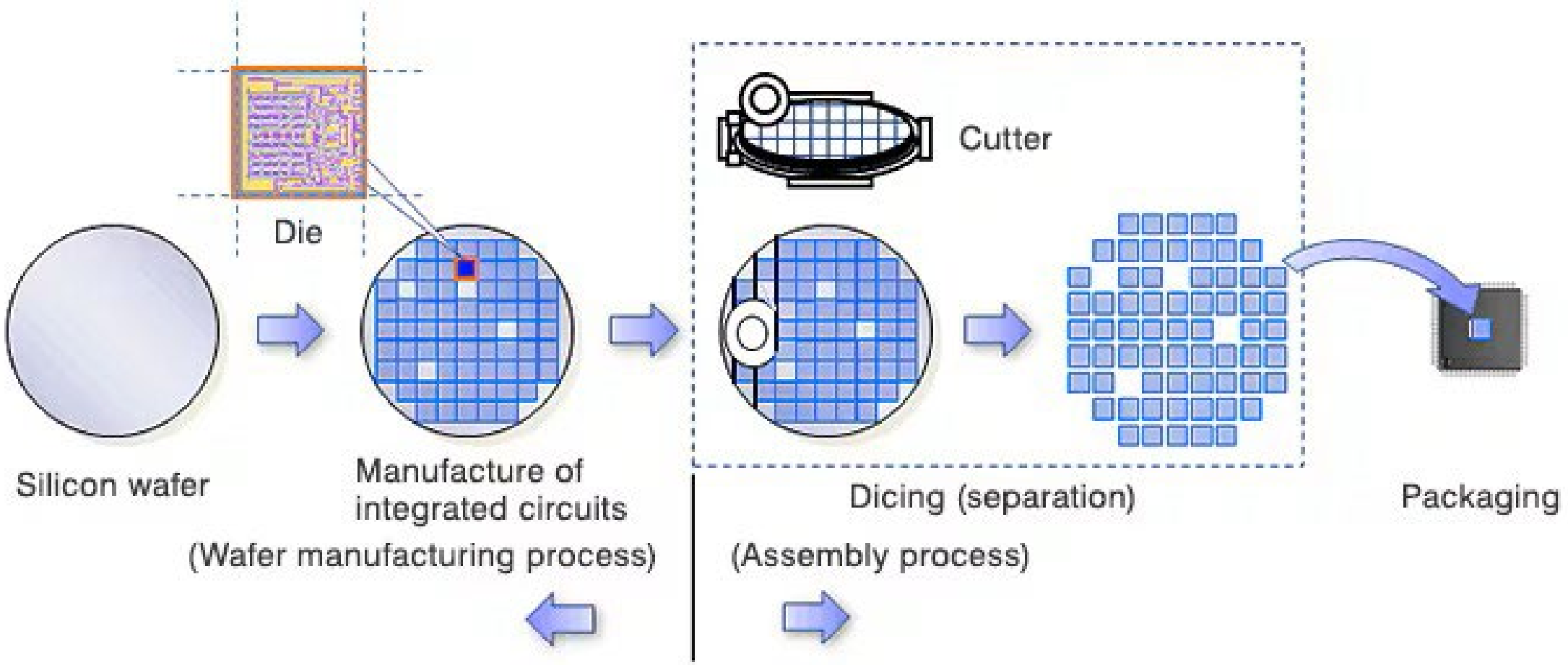
$\Rightarrow$ mostly Metalization processes

BOEL processes

Metalization processes:
deposition of metal wires and insulators



RC delay: the main factor that determines the chip's operation speed

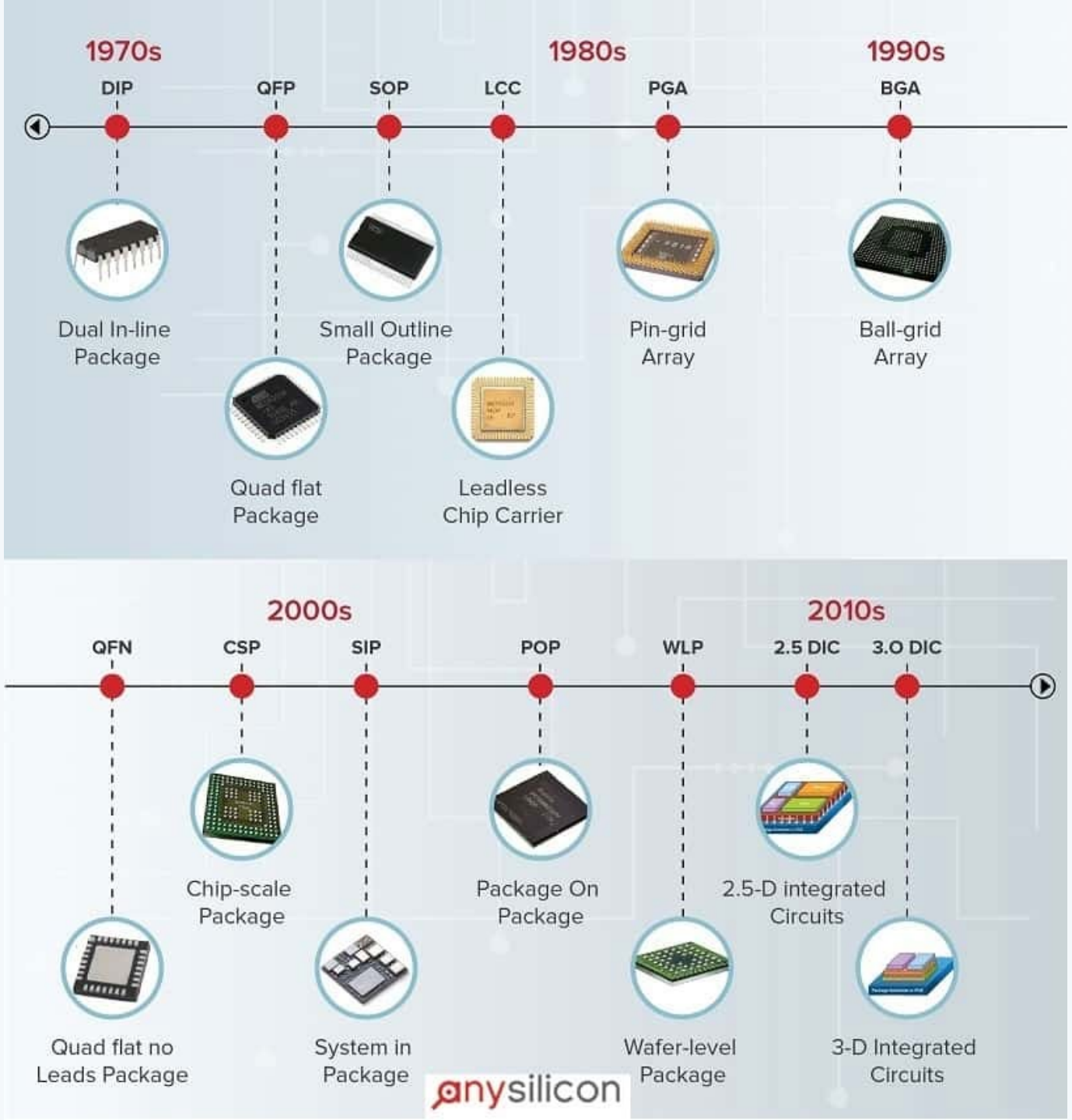


https://www.hitachi-hightech.com/global/en/media/02_il04_gif_tcm27-70428.gif

Backend processes = Assembly, Testing, Packaging (ATP)

ATP = The last production stage of semiconductor chips, where individual chips are cut from the wafers, tested, assembled, packaged, and connected with wires that can be attached to the printed circuit board (PCB). This process is often outsourced to different companies.

(https://www.semiconductors.org/wp-content/uploads/2018/09/Assembly-Packaging.pdf)



https://anysilicon.com/wp-content/uploads/2016/02/Semicondcutor-packaging-history-doubled.jpg

Summary of ATP

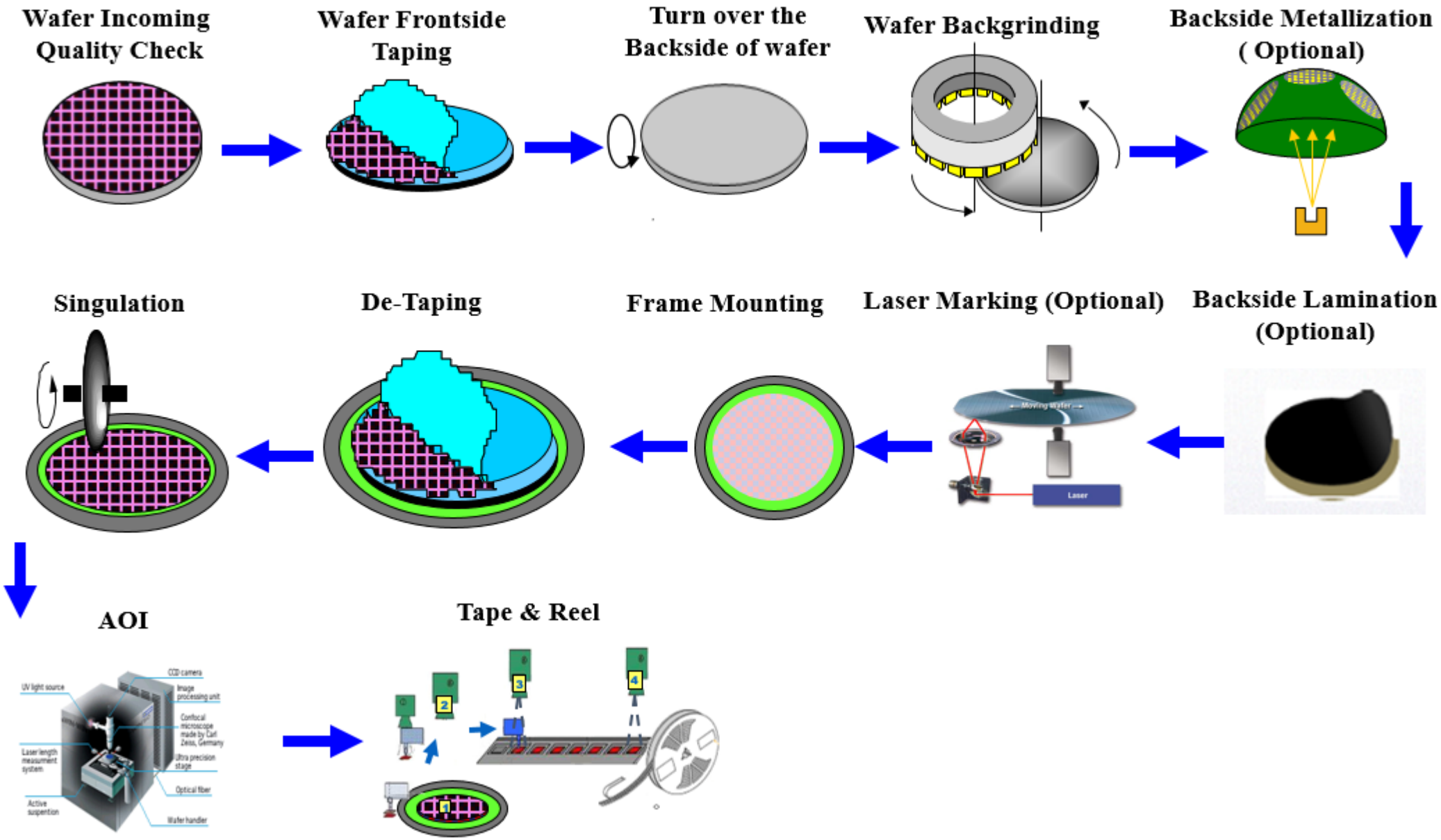
- Inspection
- Backgrinding
- Dicing
- Die bonding (die: a chip cut from a large wafer)
- Wire bonding or flip chip bonding
- molding
- Final Test

https://semi-engineers.com/process-packaging/

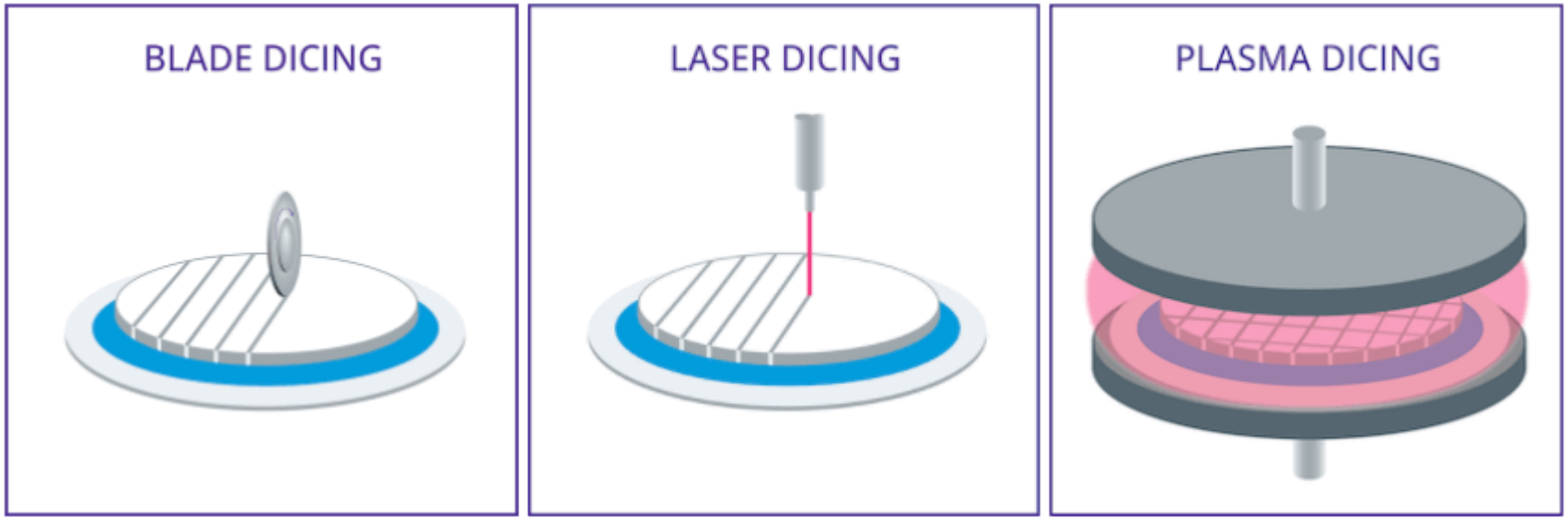
inspection

Automated inspection of a diced wafer

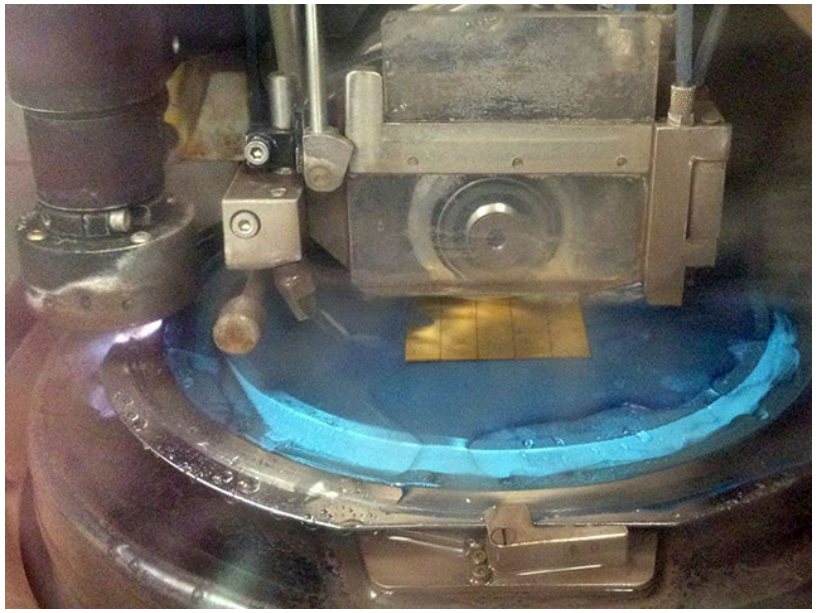
https://www.evdesignandmanufacturing.com/remote/aHR0cHM6Ly9naWVjZG4uYmxvYi5jb3JlLndpbmRvd3MubmV0L2ZpbGV1cGxvYWRzL2ltYWdlLzIwMjQvMDgvMTMvcHZhdGVwbGFfd2FmZXItc2F3aW5nLWluc3BlY3Rpb24tbWljcm9zY29wZTItLmpwZw.aorrM-ohSpw.jpg?format=webp



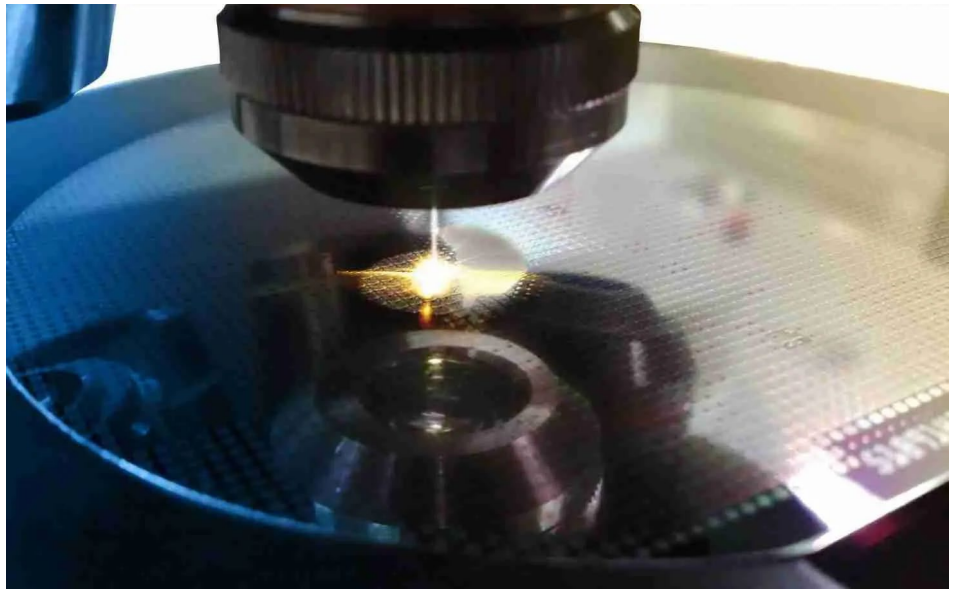
AOI: automated optical inspection



https://www.kla.com/advance/innovation/plasma-dicing-101-the-basics

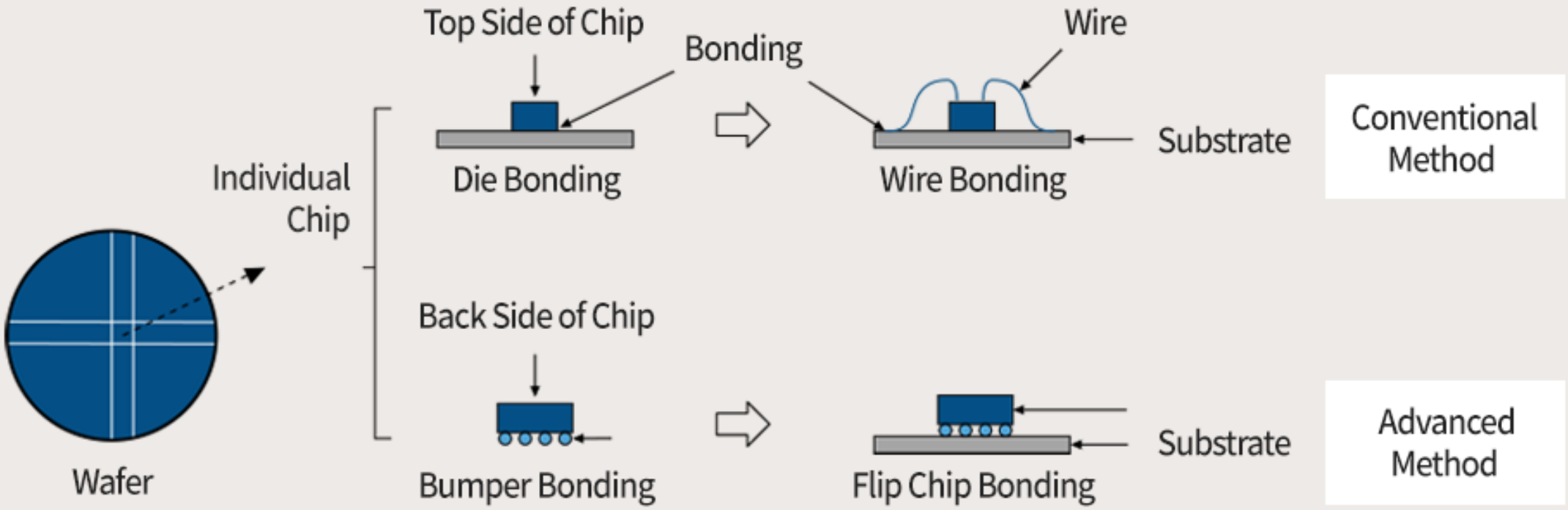


https://lnf-wiki.eecs.umich.edu/wiki/Dicing

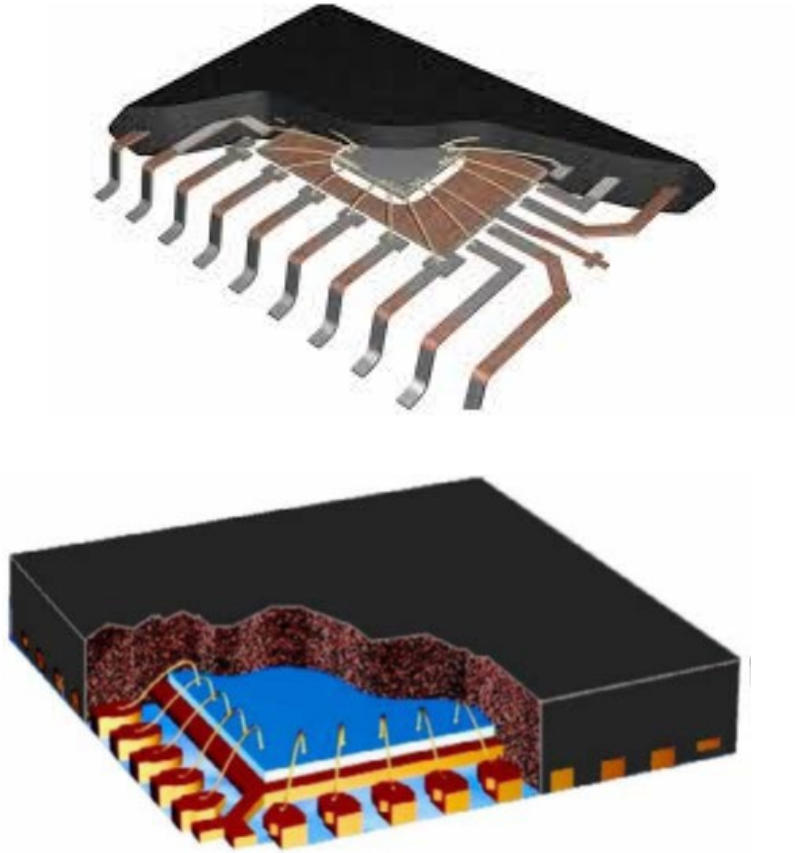


https://intech-technologies.com/introduction-to-wafer-dicing-techniques-2/

Die bonding

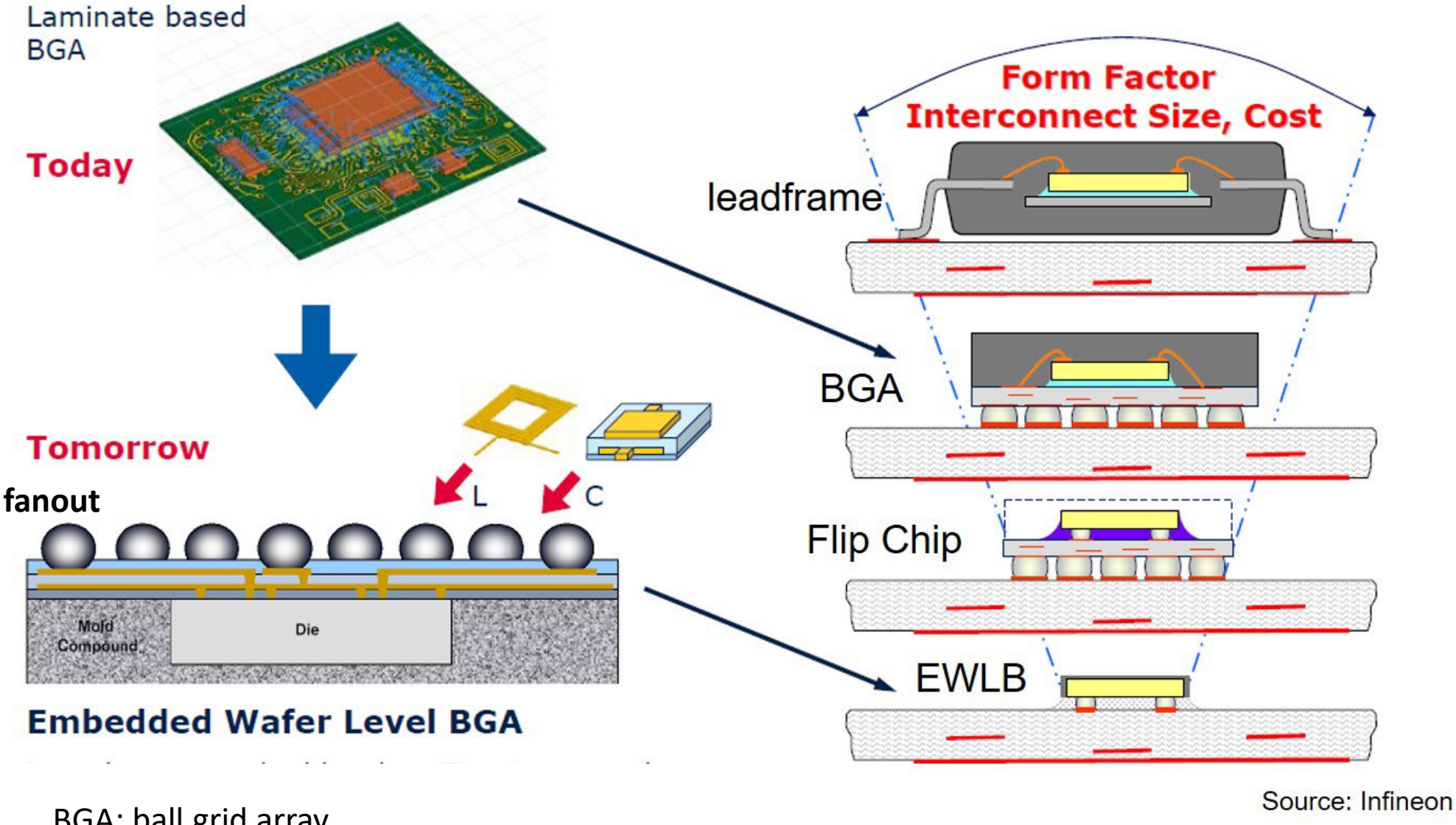

Top Side of Chip
Bonding
Wire
Individual Chip
Die Bonding
Wire Bonding
Substrate
Conventional Method
Back Side of Chip
Wafer
Bumper Bonding
Flip Chip Bonding
Substrate
Advanced Method

molding



https://prostech.vn/chip-molding-in-semiconductor/
https://polymerinnovationblog.com/polymers-electronic-packaging-part-one-introduction-mold-compounds/

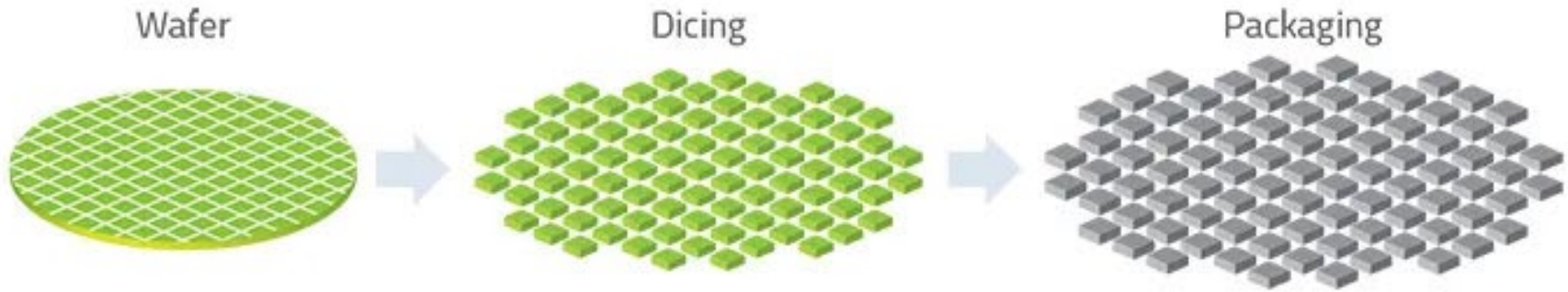
https://elimold.com/industries/semiconductor-injection-molding/



BGA: ball grid array
EWLB: embedded wafer level BGA
PBGA: plastic ball grid array

https://polymerinnovationblog.com/polymers-electronic-packaging-part-one-introduction-mold-compounds/

Traditional Packaging Process Flow



Wafer-Level Packaging Process Flow

Outline

1. The semiconductor industry
   - overview
   - technology roadmap
   - brief history
2. Outline of chip products: logic, memory, storage
3. Fundamentals of device physics
4. Fundamentals of Chip Manufacturing
   - Front-end processes (FEOL & BEOL)
   - Back-end processes
5. Summary

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Summary

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3. Fundamentals of device physics
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   - Front-end processes (FEOL & BEOL)
   - Back-end processes
5. Summary

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